

# 2010.04.07 MV Schematic

## TABLE OF CONTENTS

### MB

P02 : SYSTEM BLOCK DIAGRAM  
P03 : CLOCK MAP  
P04 : POWER DELIVERY CHART  
P05 : POWER SEQUENCY DIAGRAM  
P06 : POWER SEQUENCE CHART  
P07 : SMBUS&I2C MAP  
P08 : SlG4 HT I/F & PWR  
P09 : SlG4 CTRL & DEBUG  
P10 : SlG4 DDRIII MEMORY I/F  
P11 : RS880M-PCIE/HT LINK/SPMEM  
P12 : RS880M-SYSTEM I/F  
P13 : RS880M-POWER  
P14 : SB820M-PCIE/CPU/LPC/STRAP  
P15 : SB820M-GPIO/USB/AZ//SATA  
P16 : SB820M-POWER & DECOUPLING  
P17 : DDR3(SO-DIMM\_0/1)  
P18 : VGA\_S3 (PCI-E) 1/3  
P19 : VGA (IO)/(STRAP) 2/3  
P20 : VGA\_S3 (POWER) 3/3  
P21 : VRAM (DDR3)  
P22 : EC+KBC (IT8502E) & ROM  
P23 : Audio (CODEC\_ALC270A)

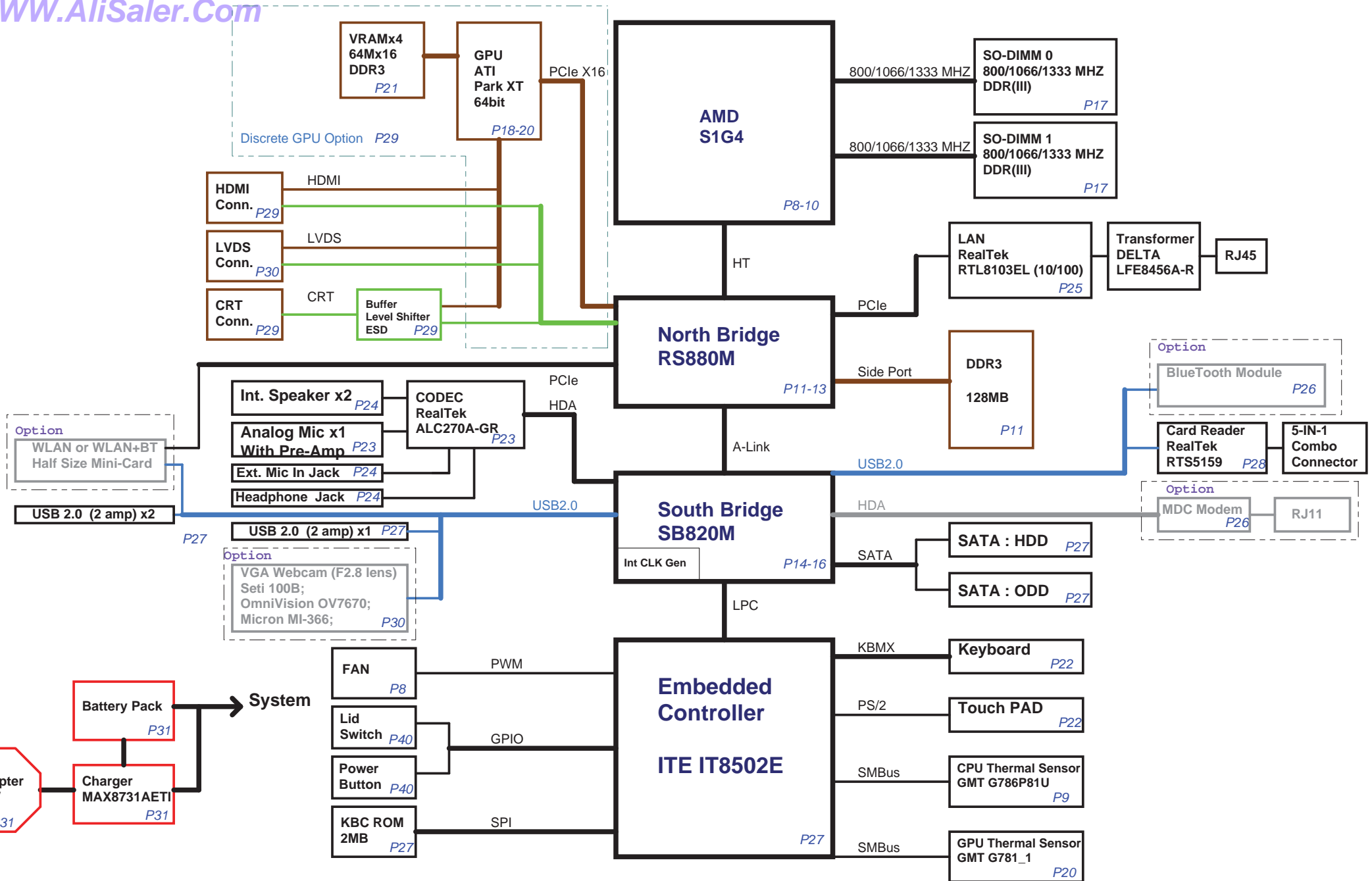
P24 : Audio (JACK+AMP+SPK+Mute)  
P25 : LAN(RTL8103EL)  
P26 : Mini PCIE & RJ11 & BT  
P27 : USBX2/USB DB/SATA CONN.  
P28 : Card Reader  
P29 : HDMI & CRT  
P30 : LVDS&Webcam  
P31 : PWR\_Charger MAX8731AETI  
P32 : 5V/3.3V SN0608098RHBT  
P33 : Vcore MAX17480  
P34 : +V1.1S TPS51117 & VDDR  
P35 : +V1.8S RT8253ALGS & VDDA  
P36 : PWR\_Others power plane  
P37 : +VCCNB & 1.5VDDR3 +0\_75V  
P38 : ATVDD TPS51217 & +VPCIE

P39 : Stitch CAP

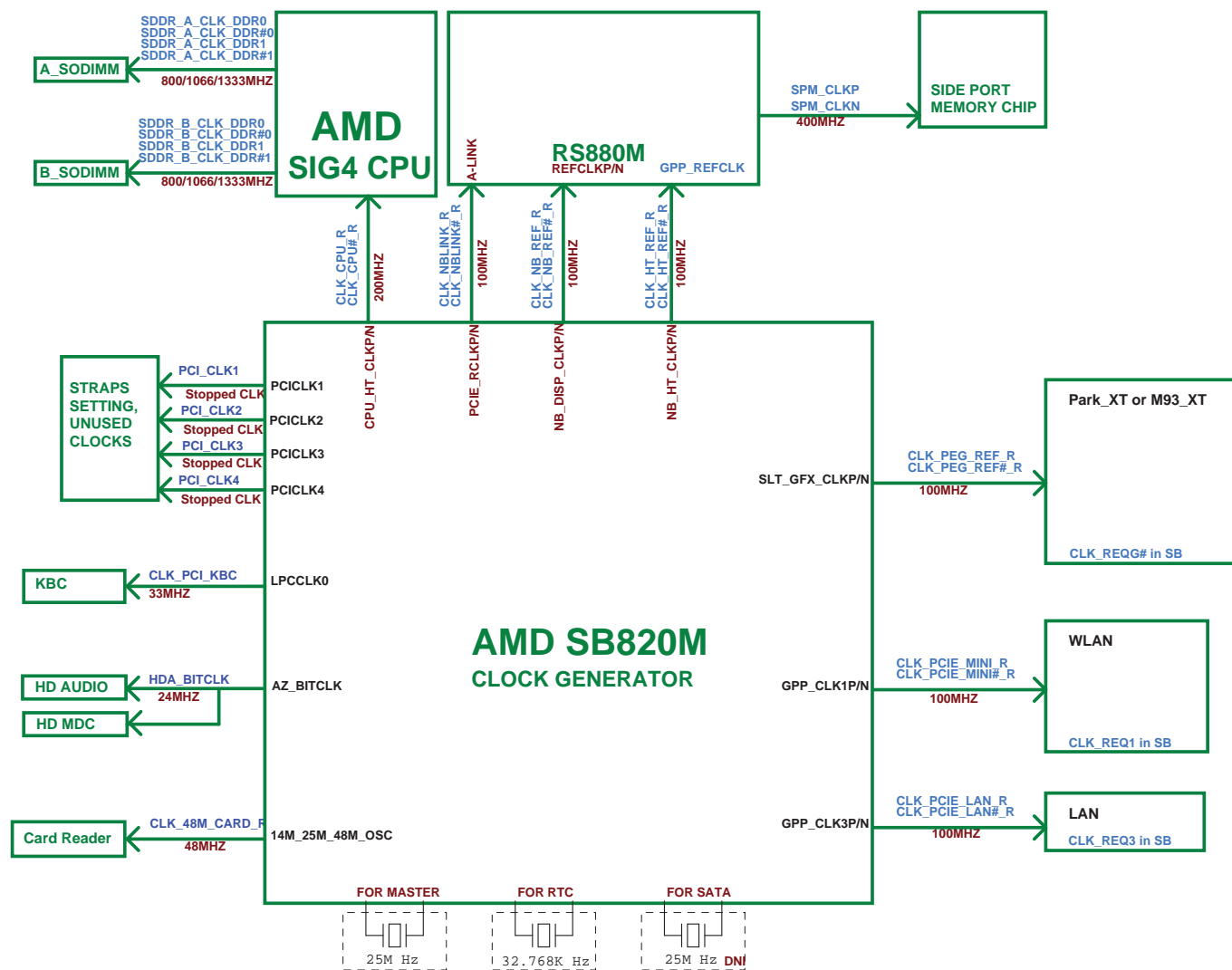
### Daughter Board

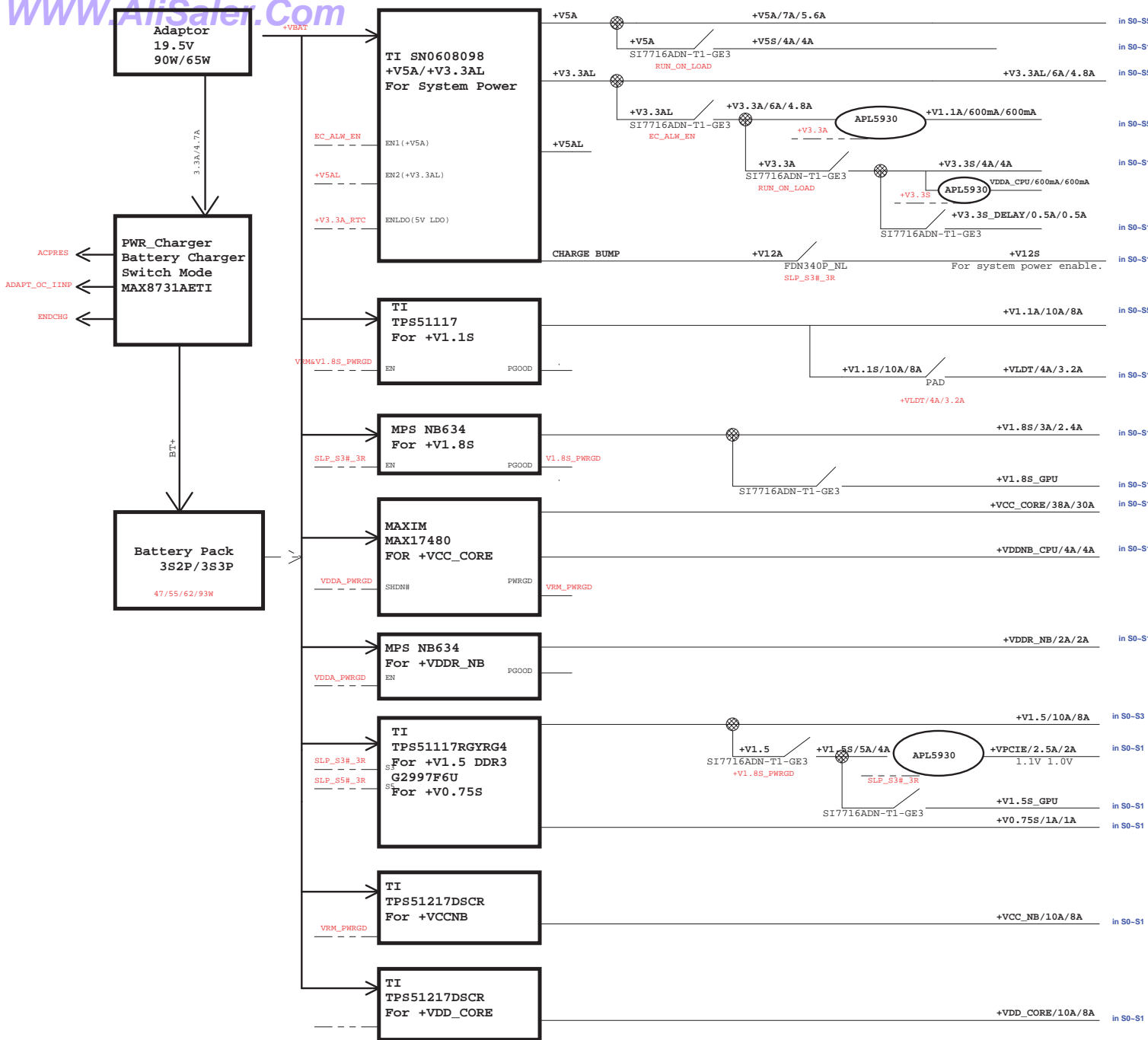
P40 -- Power Board / USB Board / SW Board

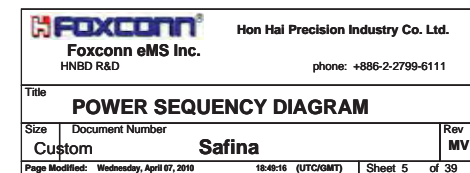
P. Leader	Check by	Design by
<b>FOXCONN</b> Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D phone: +886-2-2799-6111		
Title <b>TABLE OF CONTENTS</b>		
Size Custom	Document Number <b>Safina</b>	Rev MV
Page Modified: Wednesday, April 07, 2010 18:11:12 (UTC+08:00) Sheet 1 of 39		

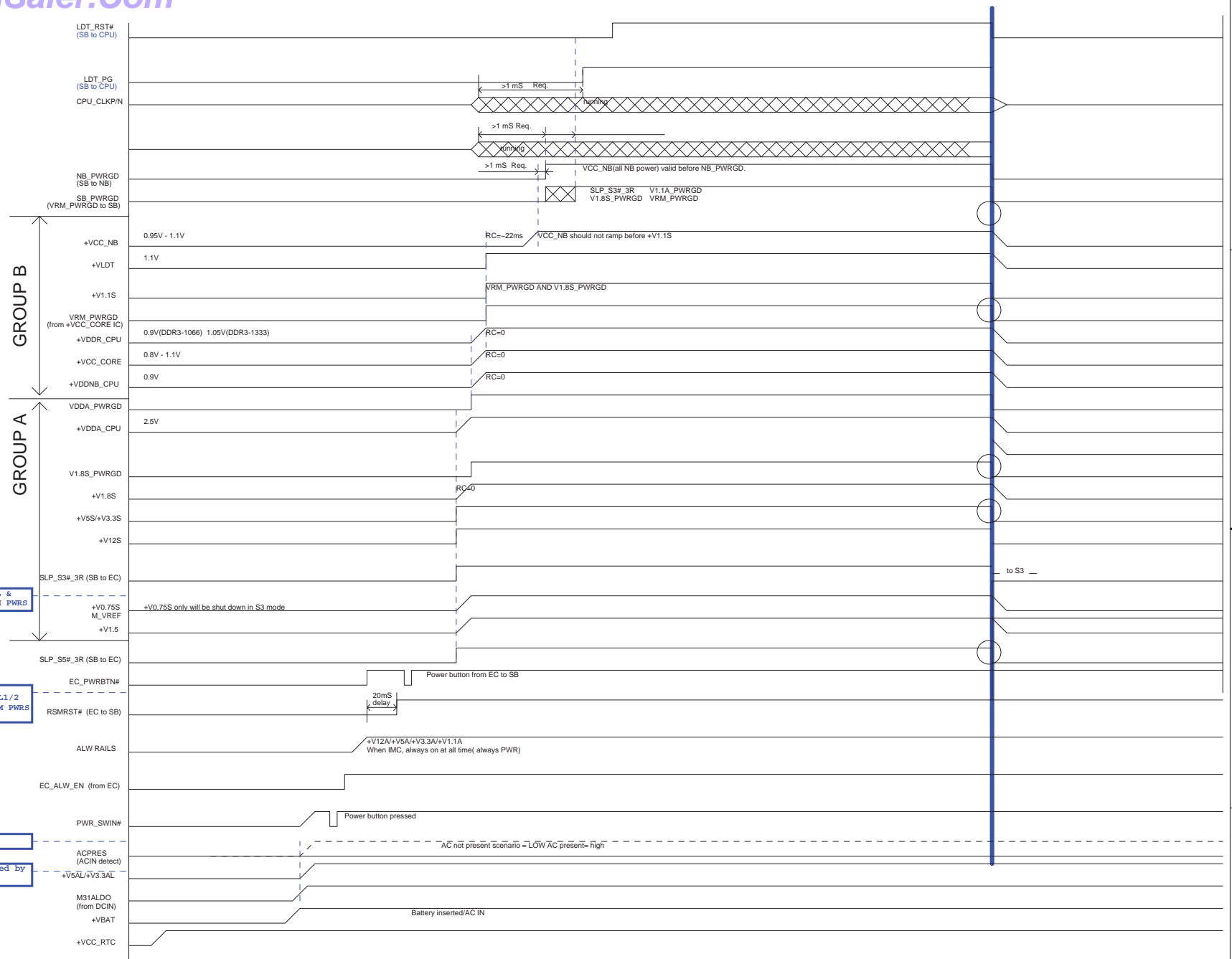


## INTERNAL CLOCK MODE

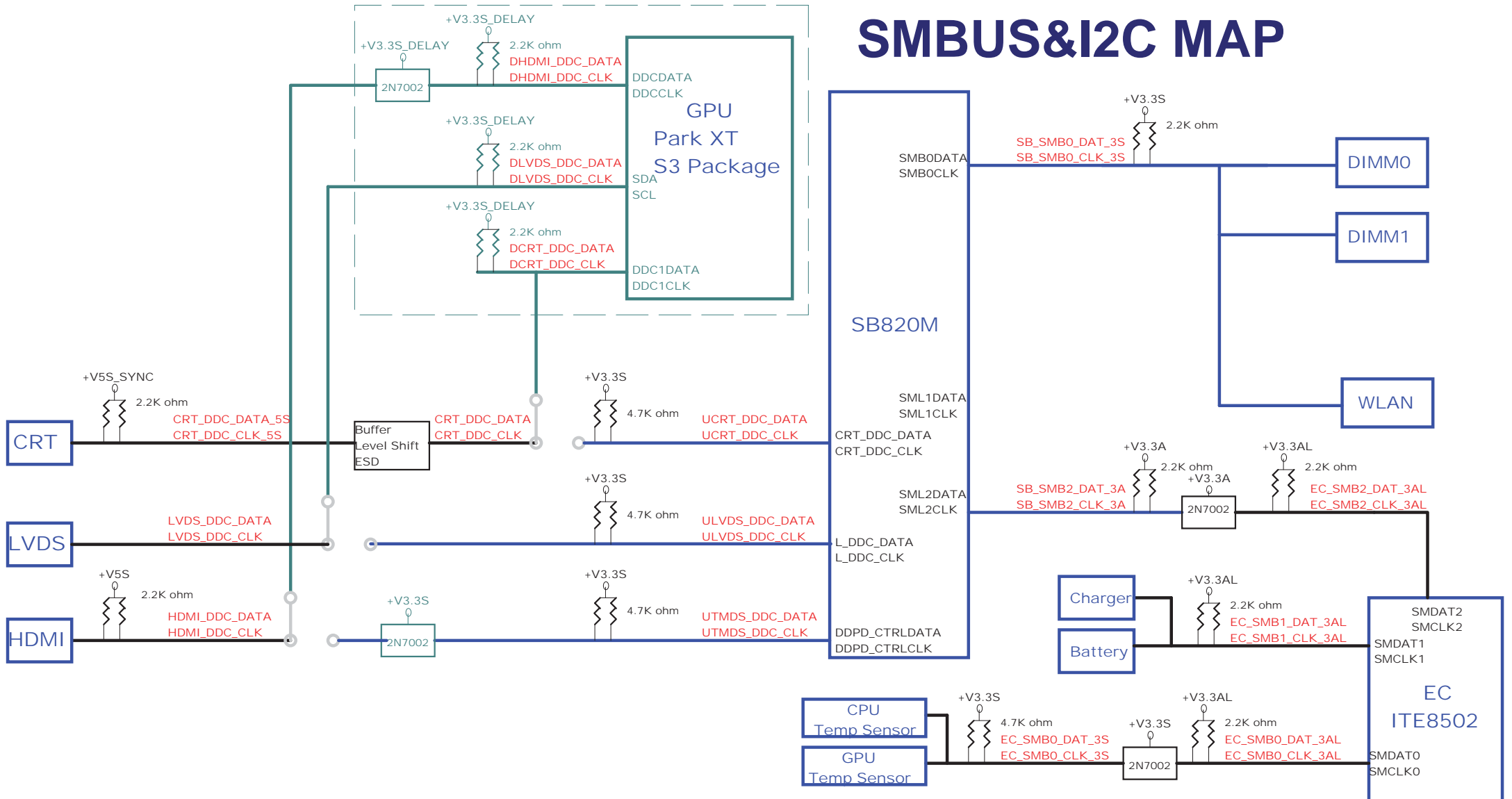






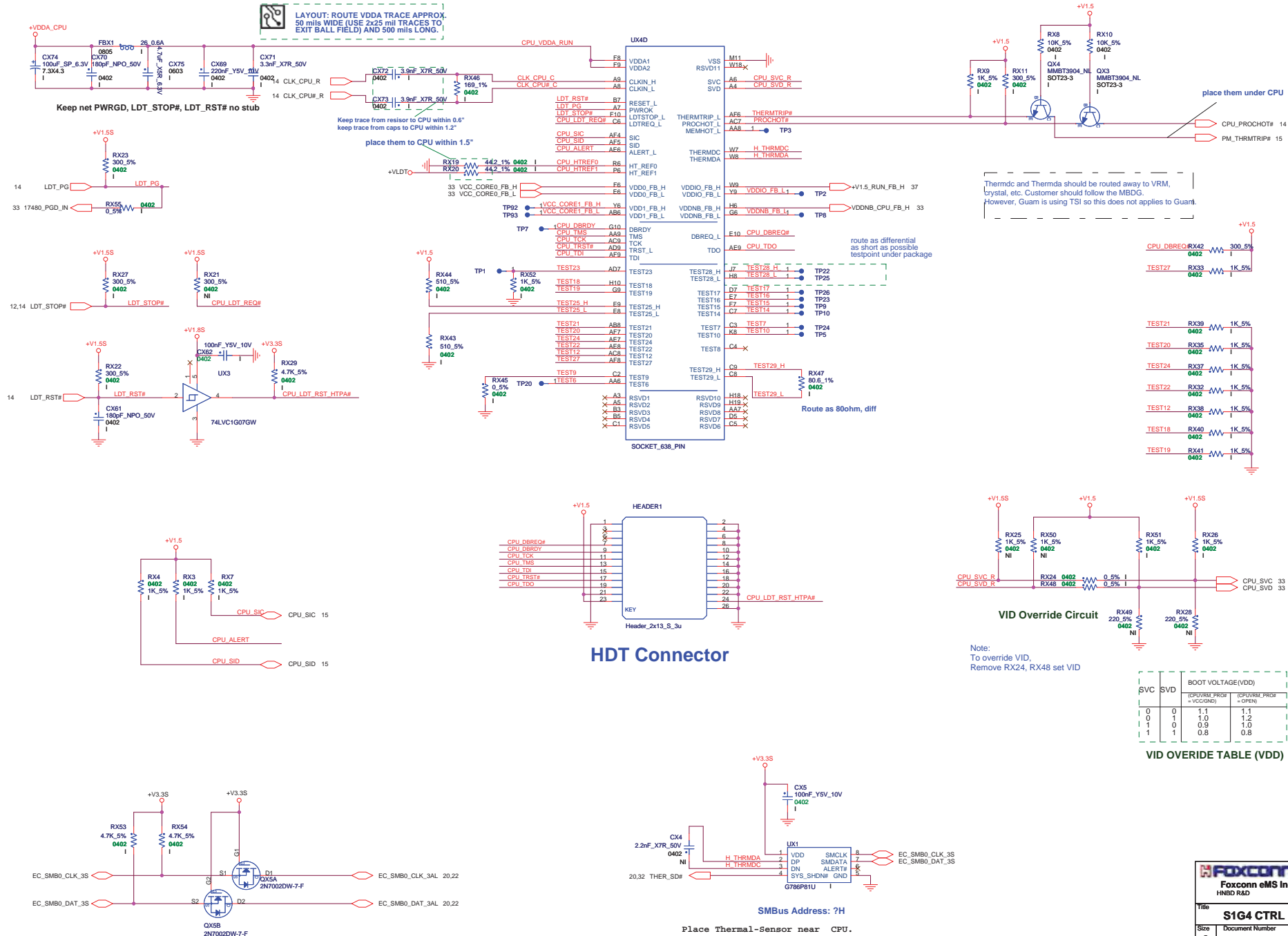


# SMBUS&I2C MAP

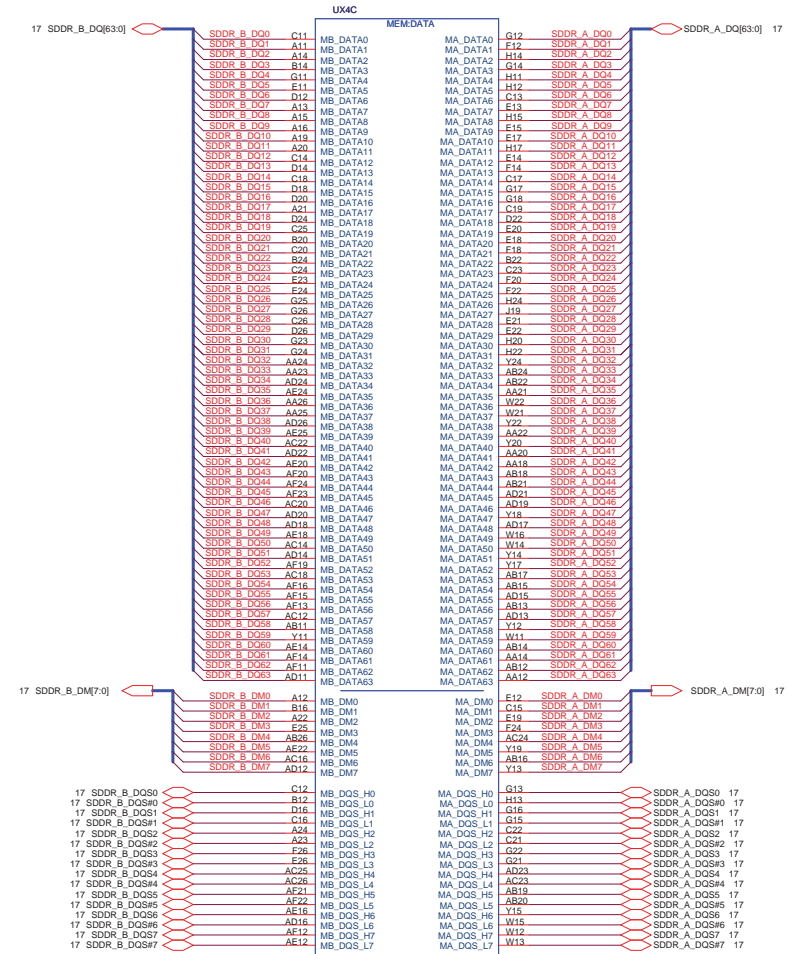
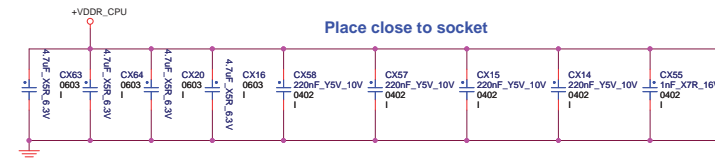
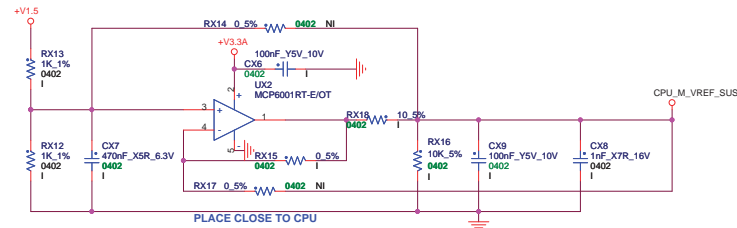
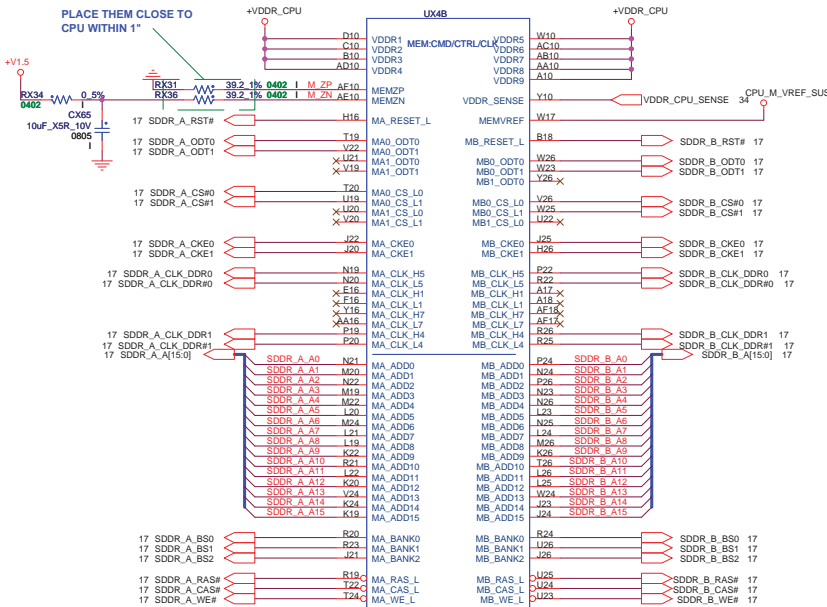








# Processor Memory Interface

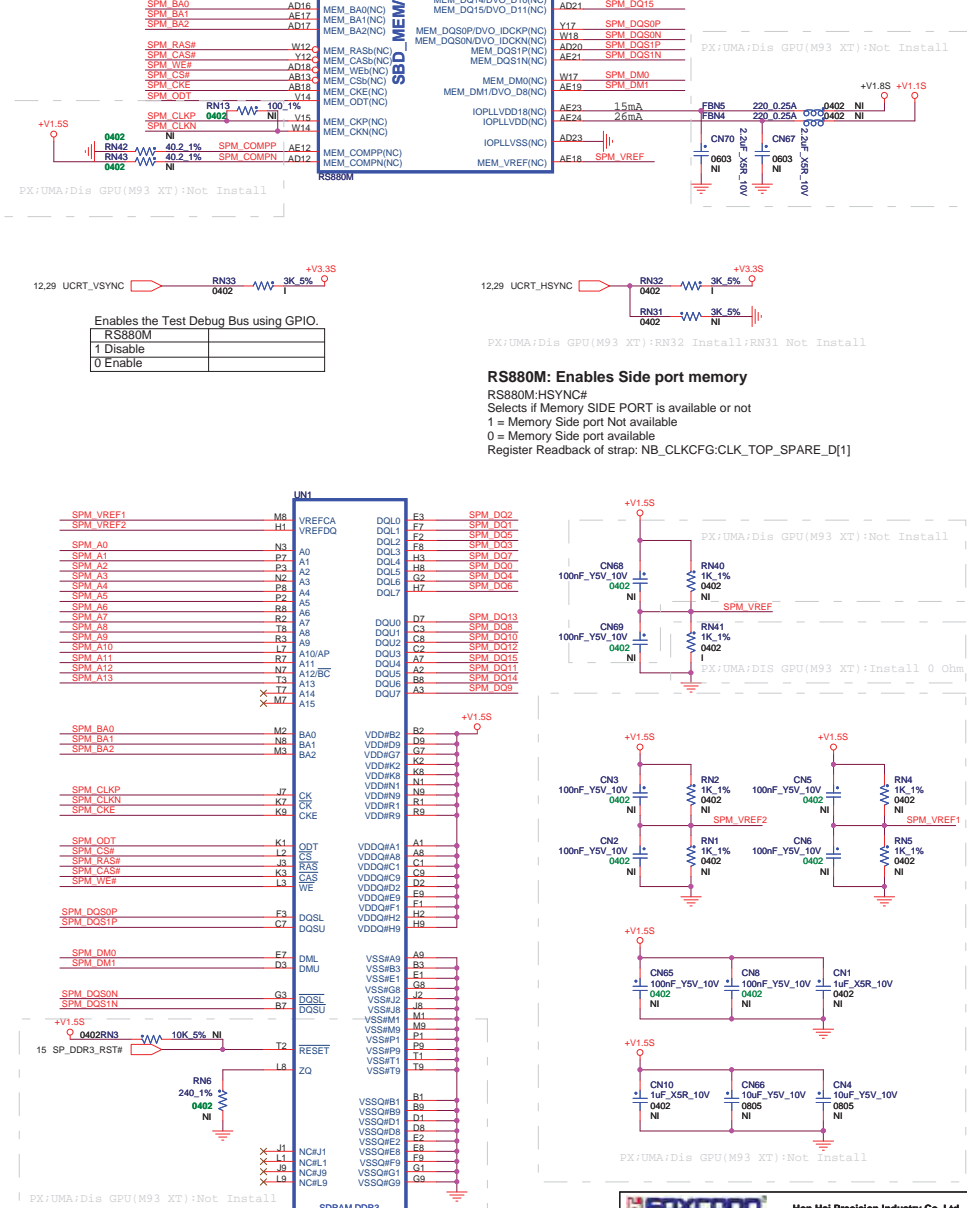
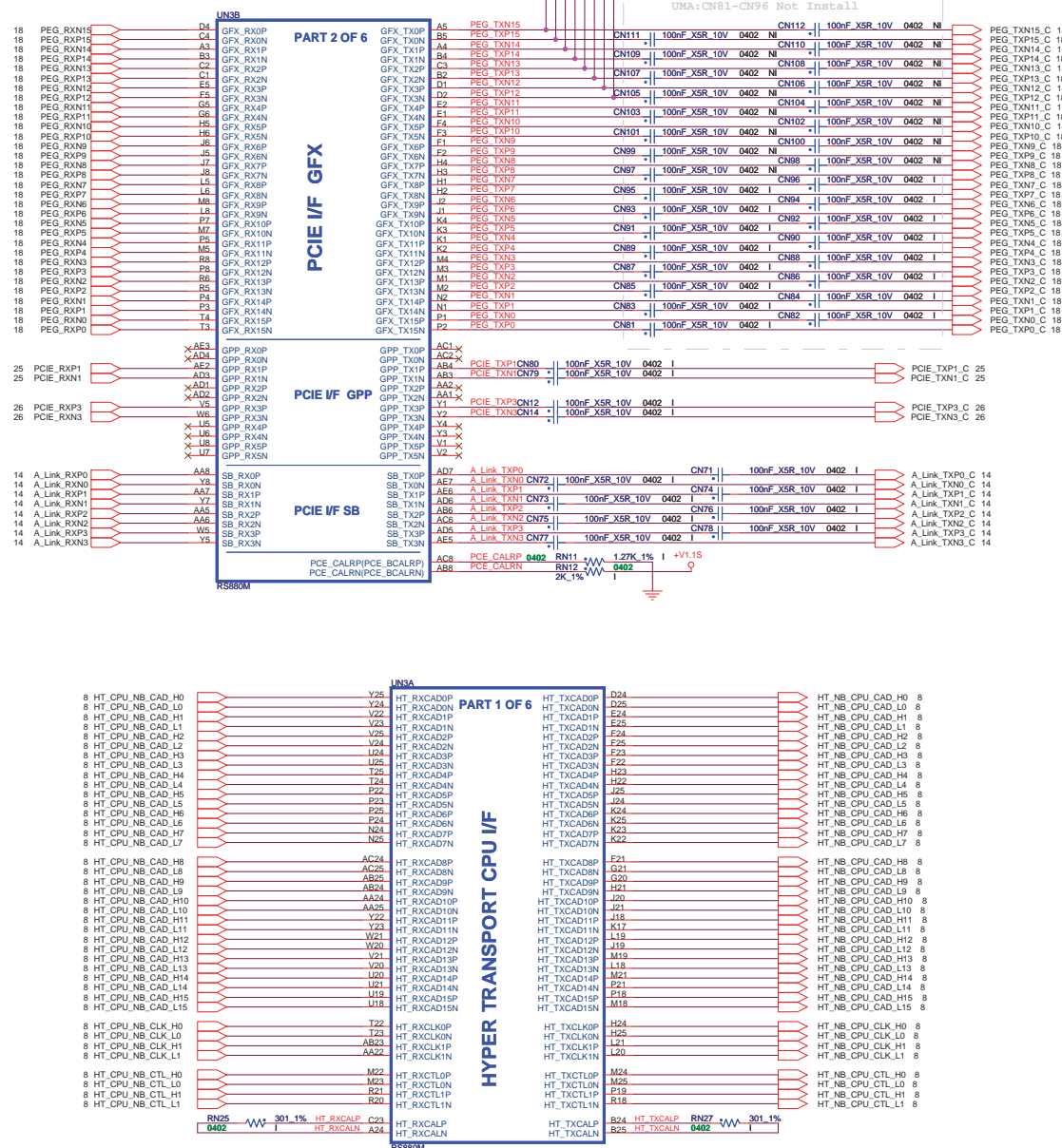


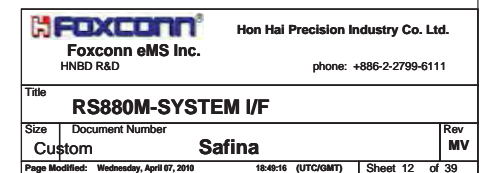


Keep the impedance of PCIe lane to 85ohm +/-15% including the A-link



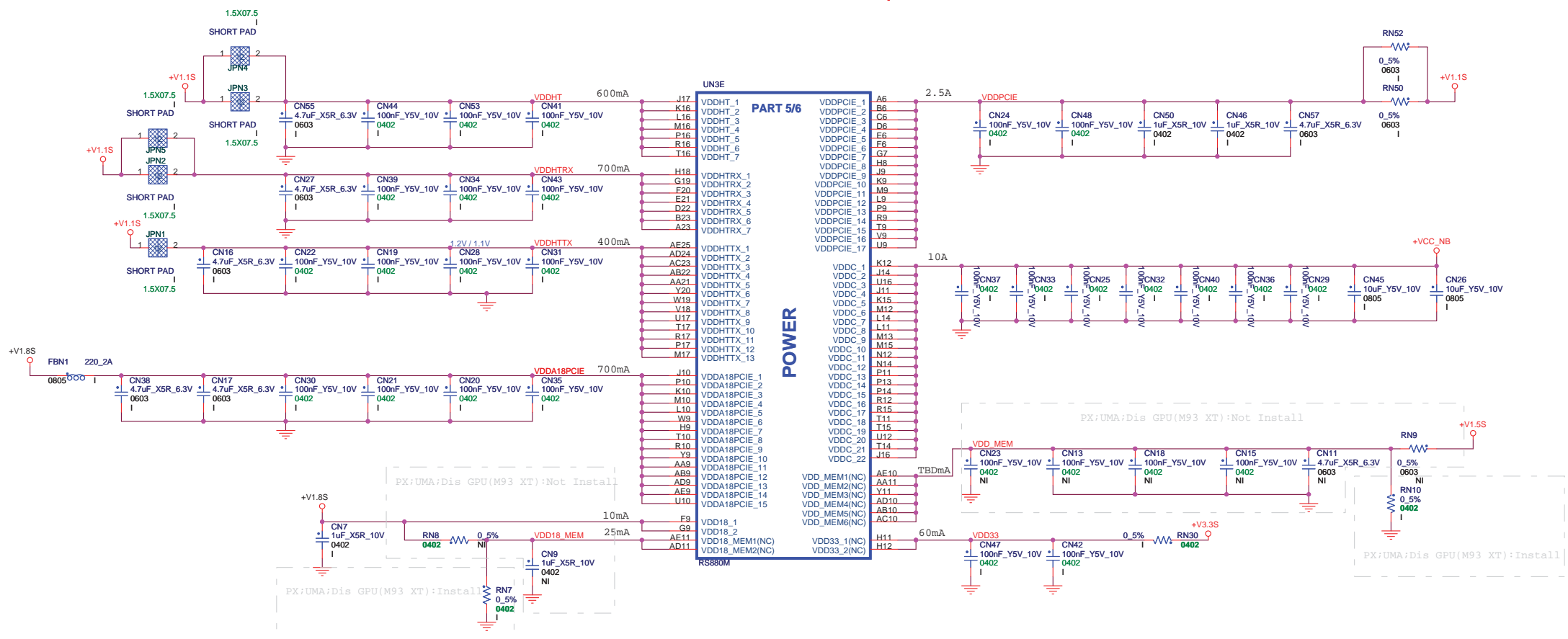
All PCIe lane should route 8" max for Gen2 connector and max 12" for Gen2 on board devices





RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC





PLACE THESE PCIE AC COUPLING CAPS CLOSE TO US1

SB800 Part 1 of 5

PCIE CLK#

PCIE RST#

PCIE CLK#

PCIE RST#

PCIE CLK#

PCIE RST#

PCIE CLK#

PCIE RST#

PCIE CLK#

PCIE RST#

PCIE CLK#

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PCIE RST#

PCIE CLK#

PCIE RST#

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PCIE RST#

PCIE CLK#

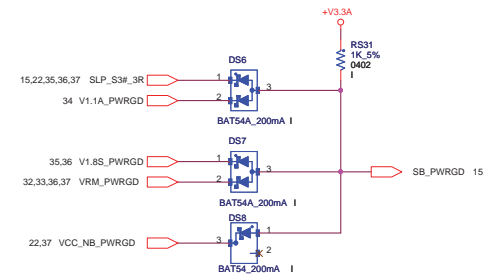
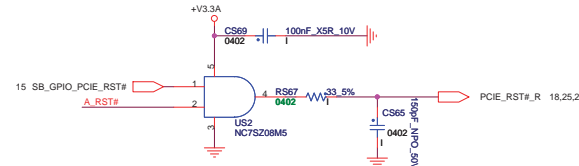
PCIE RST#

PCIE CLK#

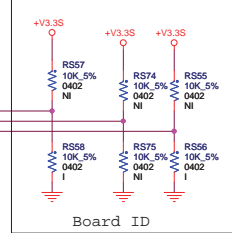
PCIE RST#

PCIE CLK#

PCIE RST#



GPIO 29/30/31	Type	Vendor	P/N
010	64M X 16 128MB	SamSung	K4W1G1646E-HC12
000	64M X 16 128MB	Hynix	H5TQ1G63BFR-12C



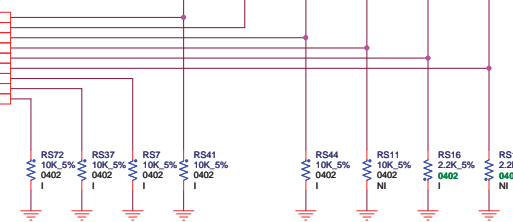
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE PCI MEM BOOT

REQUIRED STRAPS

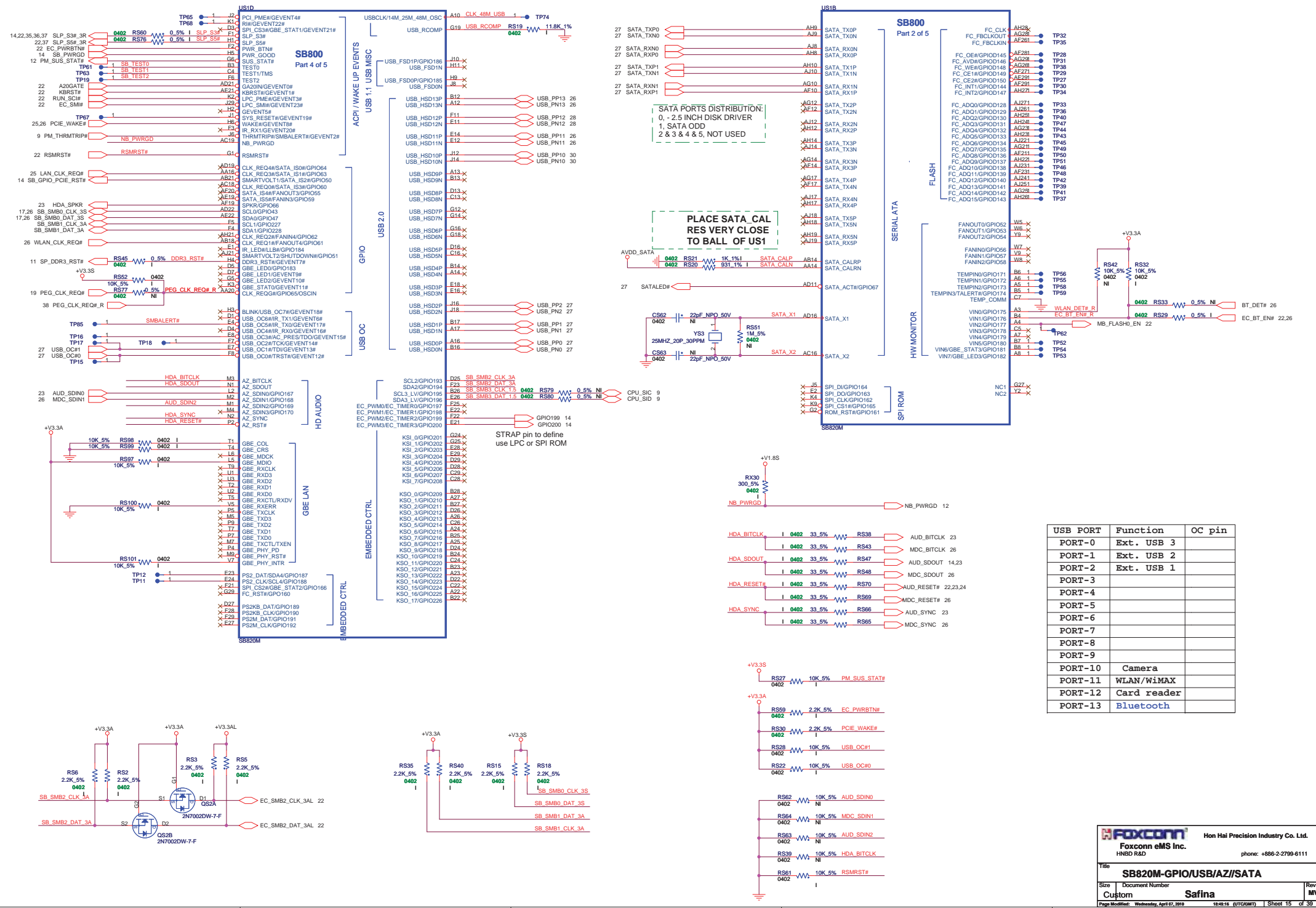


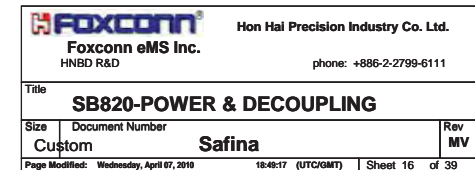
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

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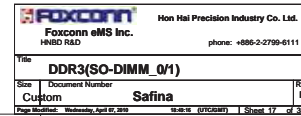
Title: **SB820M-PCIE/CPU/LPC/STRAP**

Size: Document Number  
Custom: Safina  
Page Modified: Wednesday, April 27, 2011 10:45:15 (UTC/GMT) Sheet 14 of 39

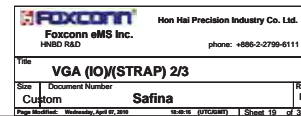


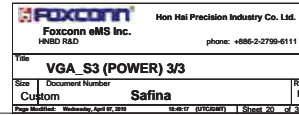


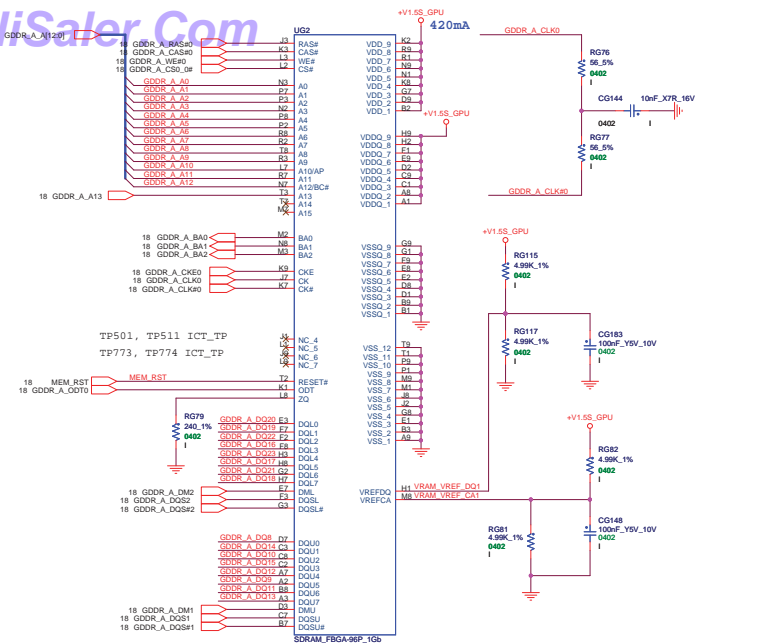




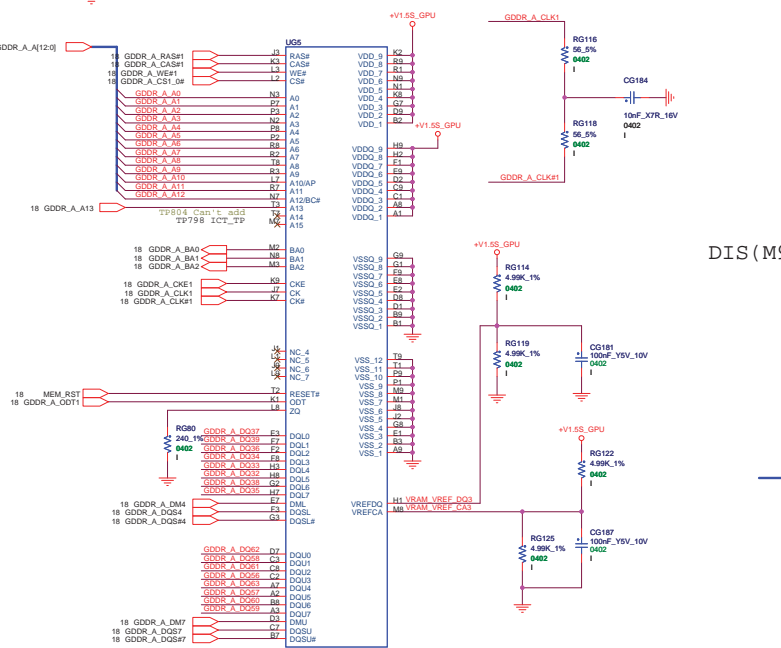
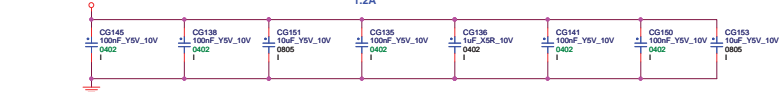




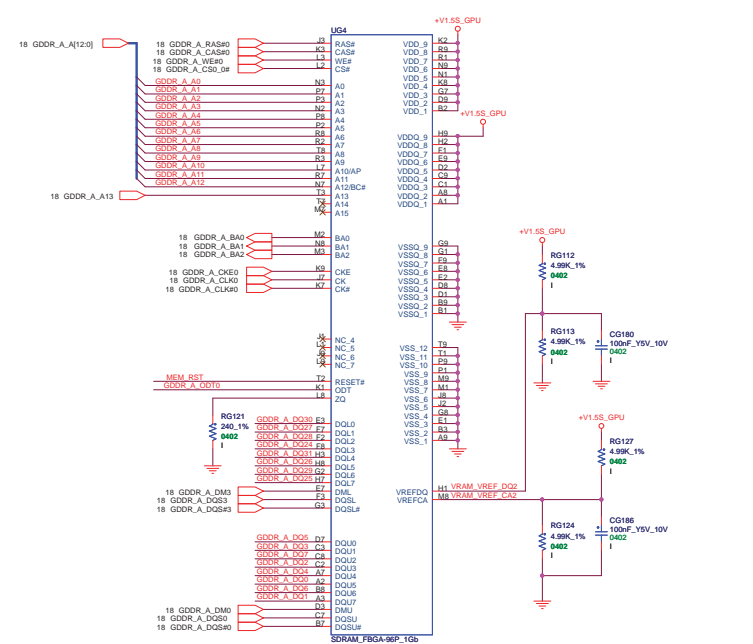
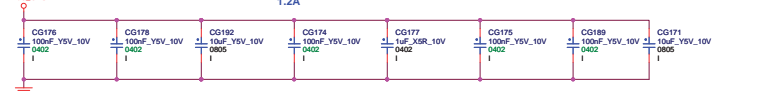




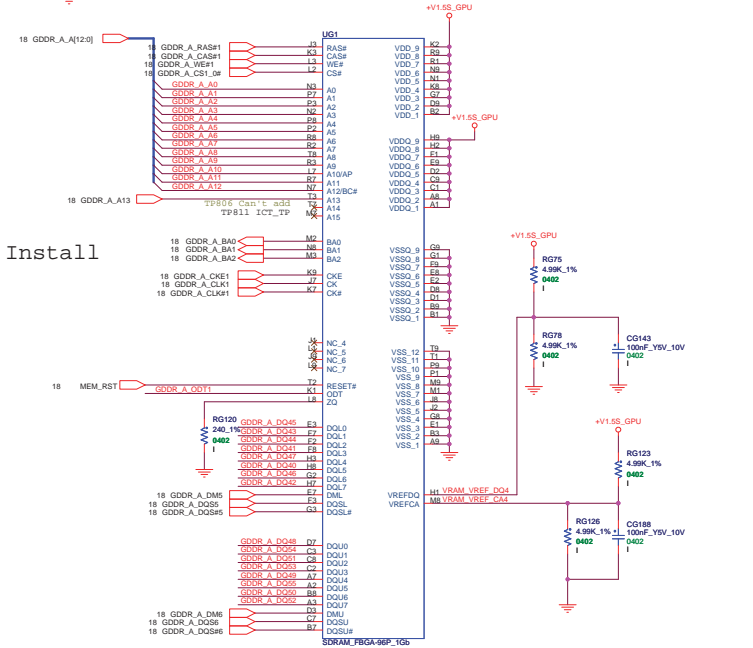
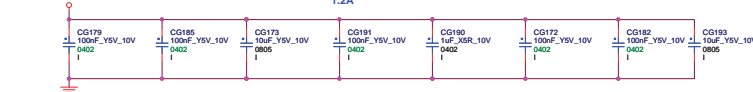
Place around the VRAM UG2



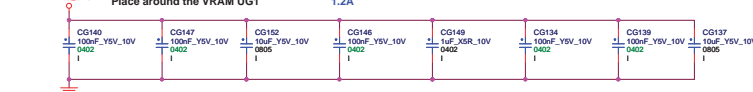
**Place around the VRAM UG5**



Place around the VRAM UG4

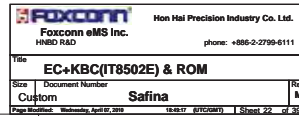


Place around the VRAM UIC1

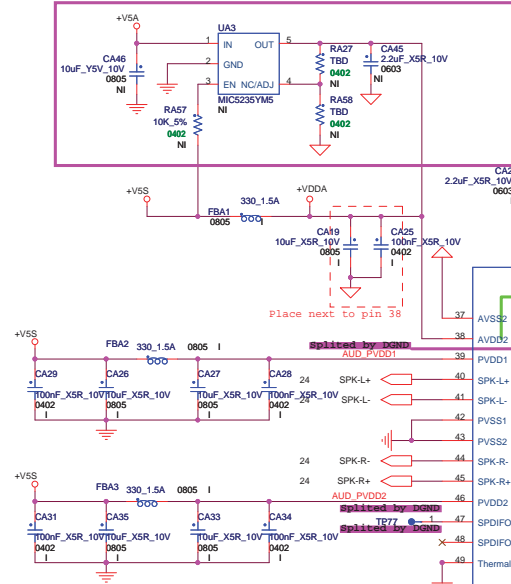


DIS(M93 XT);PX : Install





Reserved LDO circuitry for +VDDA power source



Place next to pin 38

Split by DDD

Split by DDD

Split by DDD

Split by DDD

Split by DDD

Split by DDD

Split by DDD

Split by DDD

Split by DDD

Split by DDD

Split by DDD

Split by DDD

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Split by DDD

Split by DDD

Split by DDD

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Split by DDD

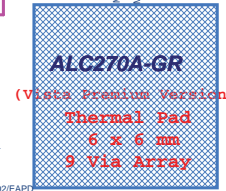
Split by DDD

Split by DDD

Split by DDD

Split by DDD

Split by DDD



ALC270A-GR  
(Vista Premium Version)  
Thermal Pad  
6 x 6 mm  
9 Via Array

ANALOG

DIGITAL  
(Include Thermal pad)

HDA\_SPKR\_R\_C

HDA\_SPKR\_R

HDA\_SPKR\_R

HDA\_SPKR\_R

HDA\_SPKR\_R

HDA\_SPKR\_R

HDA\_SPKR\_R

HDA\_SPKR\_R

HDA\_SPKR\_R

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HDA\_SPKR\_R

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HDA\_SPKR\_R

HDA\_SPKR\_R

HDA\_SPKR\_R

PC BEEP

PC BEEP

PC BEEP

PC BEEP

PC BEEP

PC BEEP

PC BEEP

PC BEEP

PC BEEP

PC BEEP

PC BEEP

PC BEEP

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PC BEEP

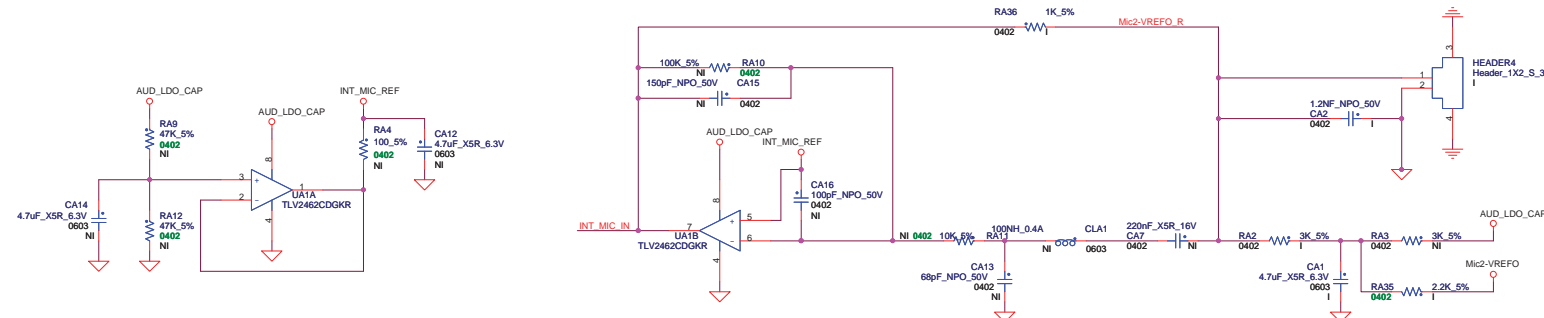
PC BEEP

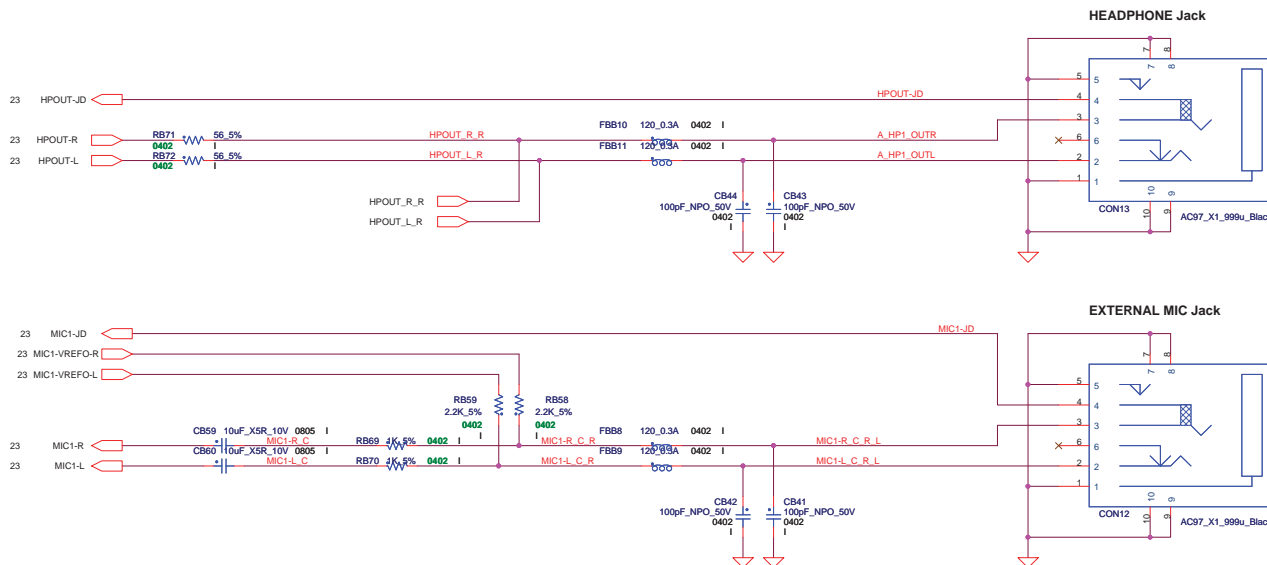
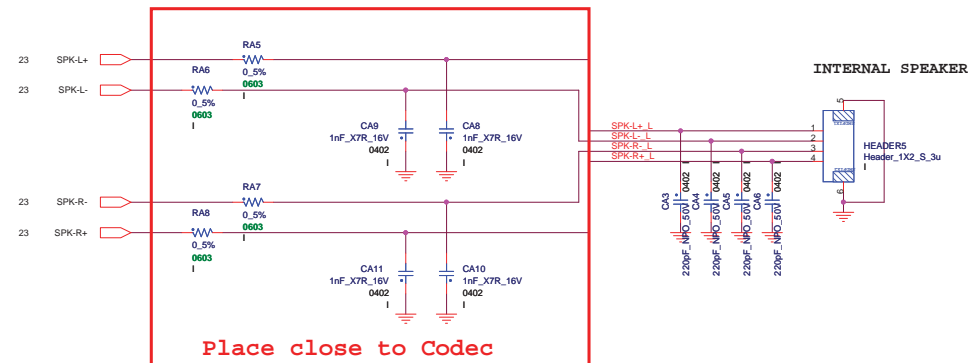
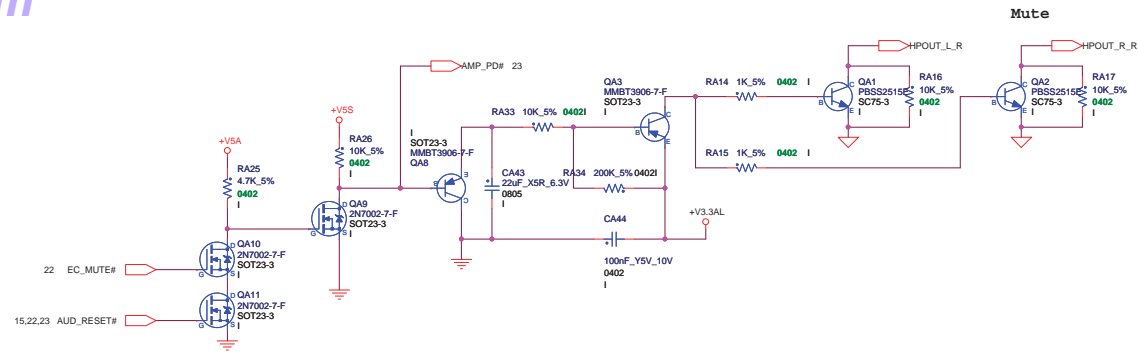
PC BEEP

PC BEEP

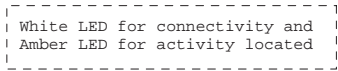
<<Attention>>  
For power\_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :  
1. If you want the system make warning signal after power on , please let EC\_MUTE# High first.  
2. When you want to exit your Bios Programming Code, please let the EC\_MUTE# Low. (The programming is different from before . )

PD# = 0V : Power down Class D SPK amplifier  
PD# = 3.3V : Power up Class D SPK amplifier

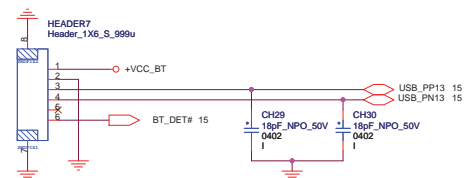
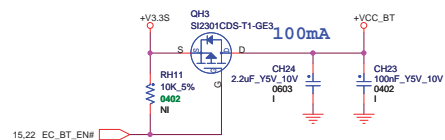
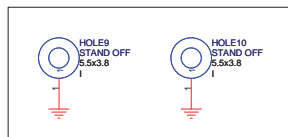






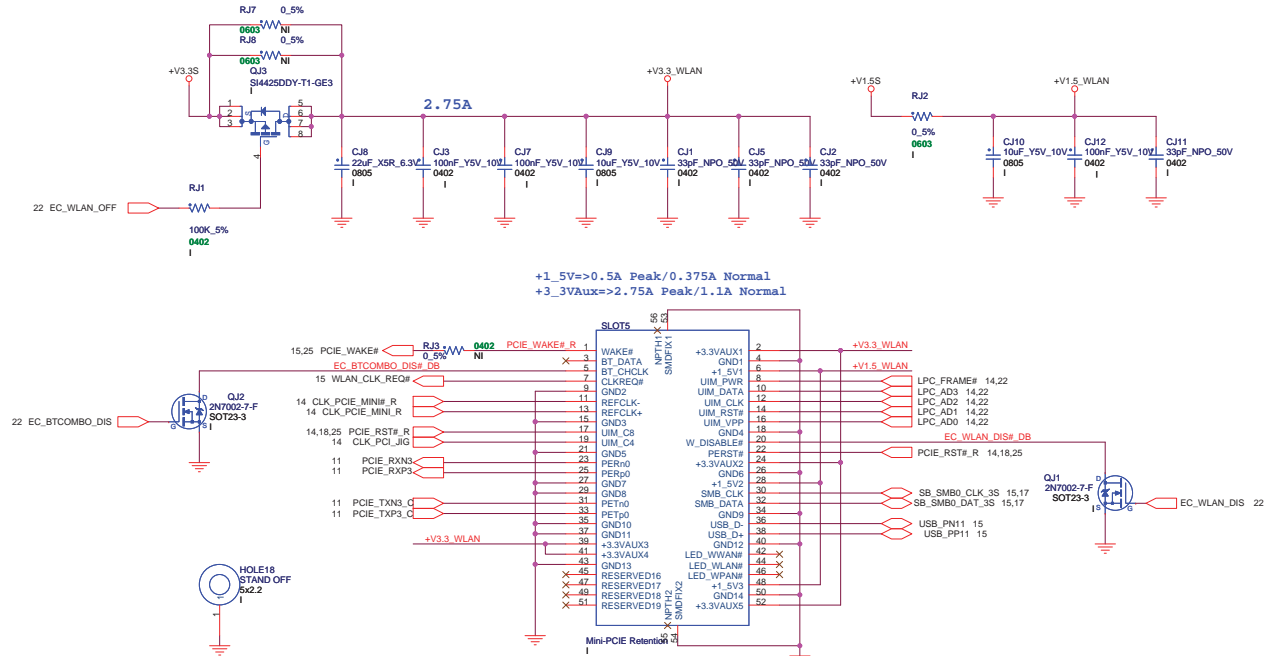
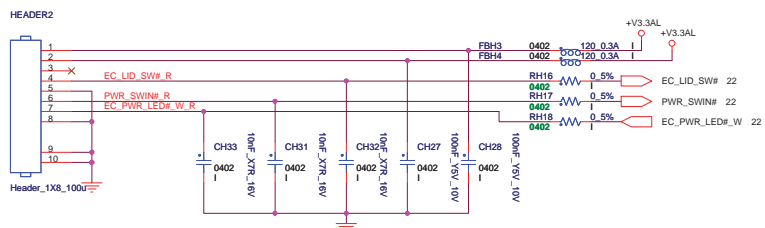


## Ethernet

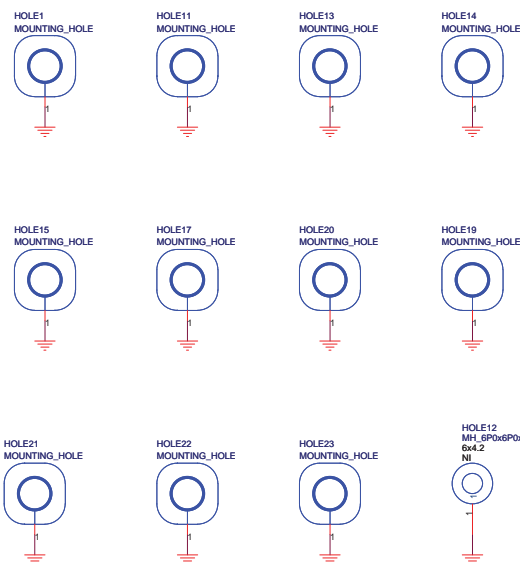


Bluetooth CONN.

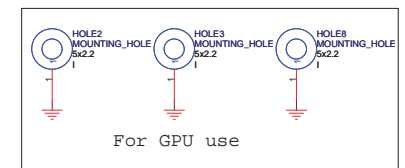
PWR Board CONN.



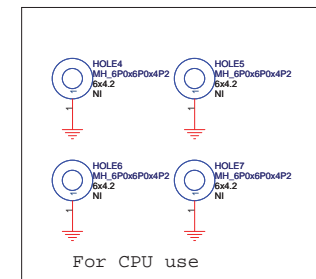
Half Mini Card for WLAN



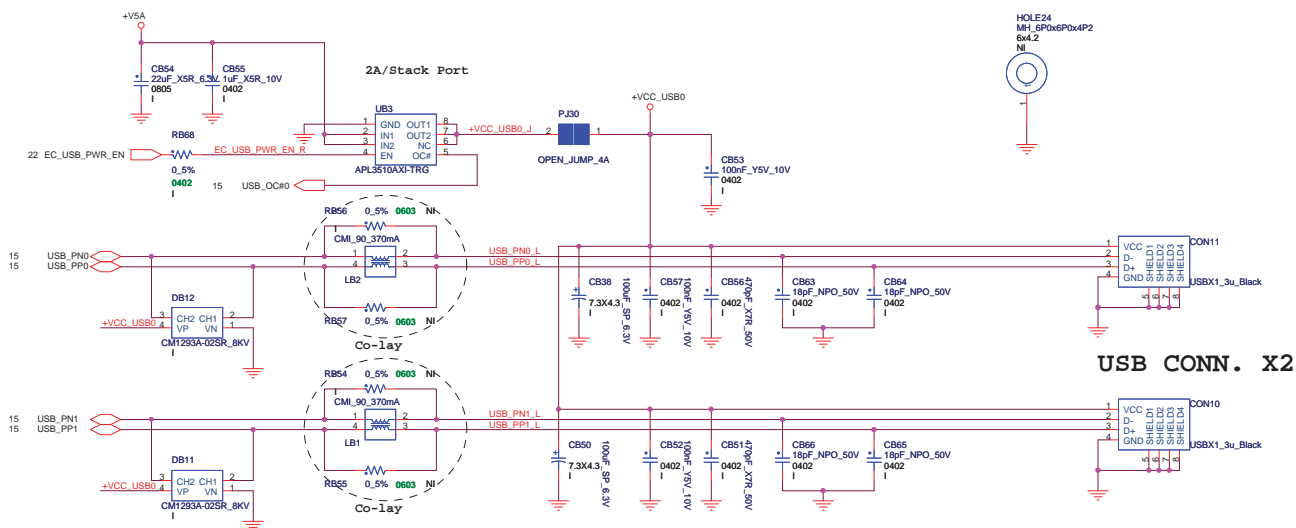
### Mounting HOLE



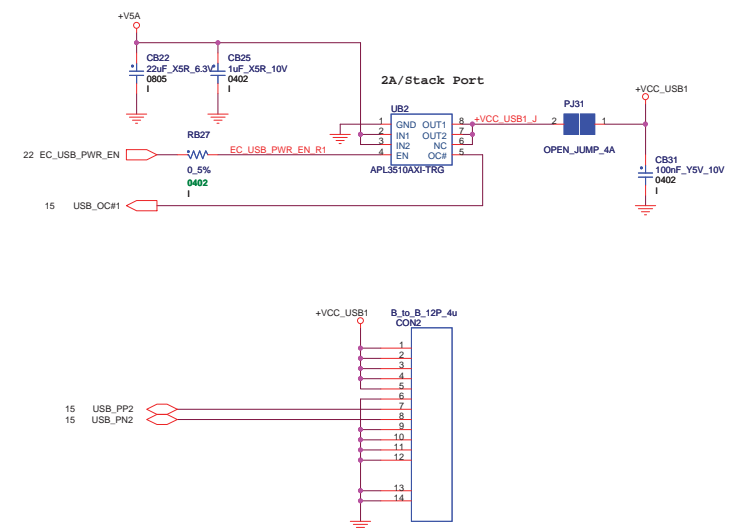
For GPU use



For CPU use

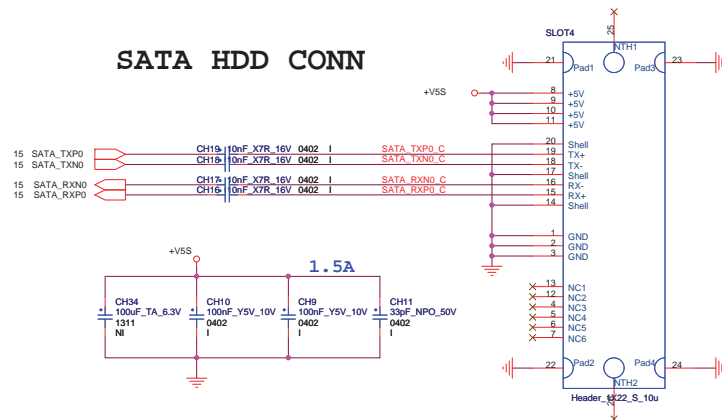


USB CONN. X2

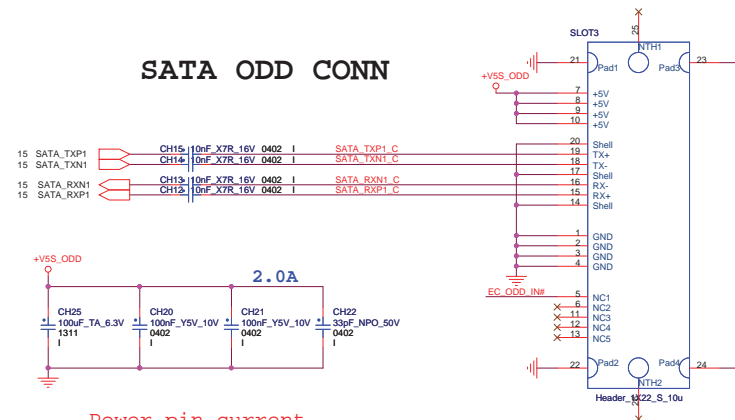


## USB Board CONN.

## SATA HDD CONN

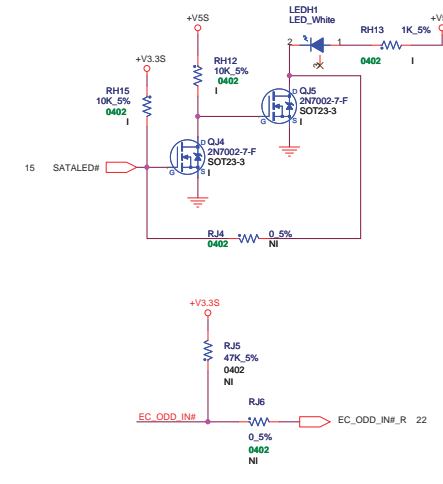


**SATA ODD CONN**

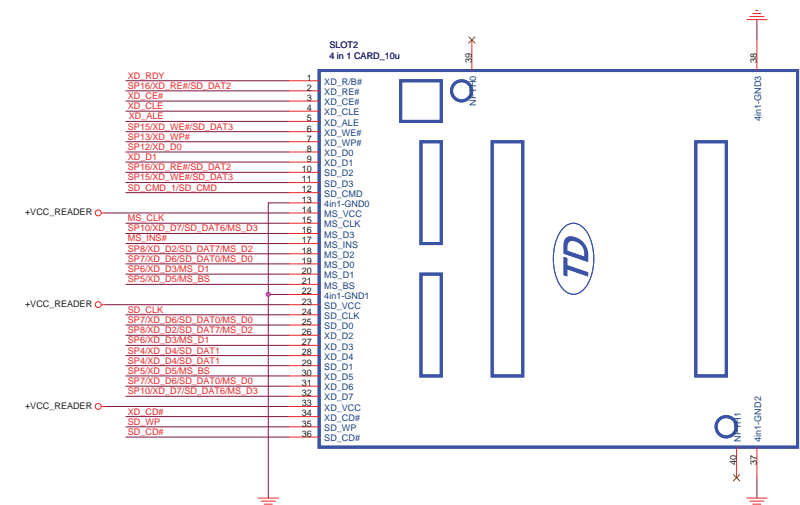
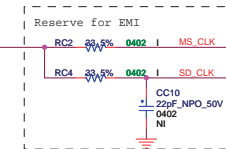
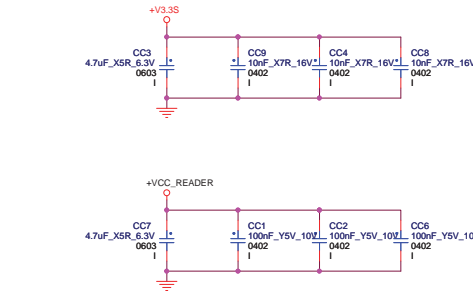
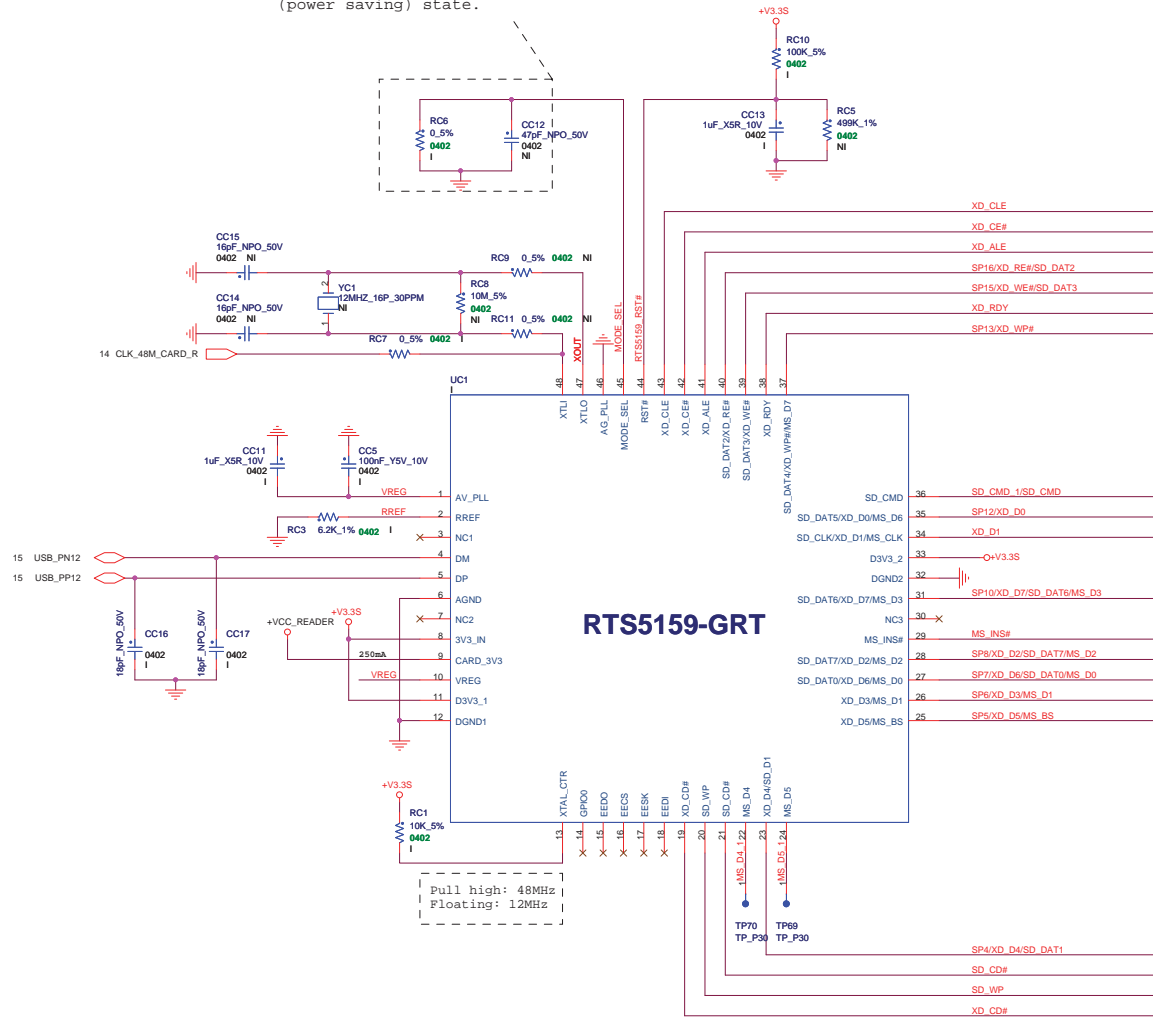


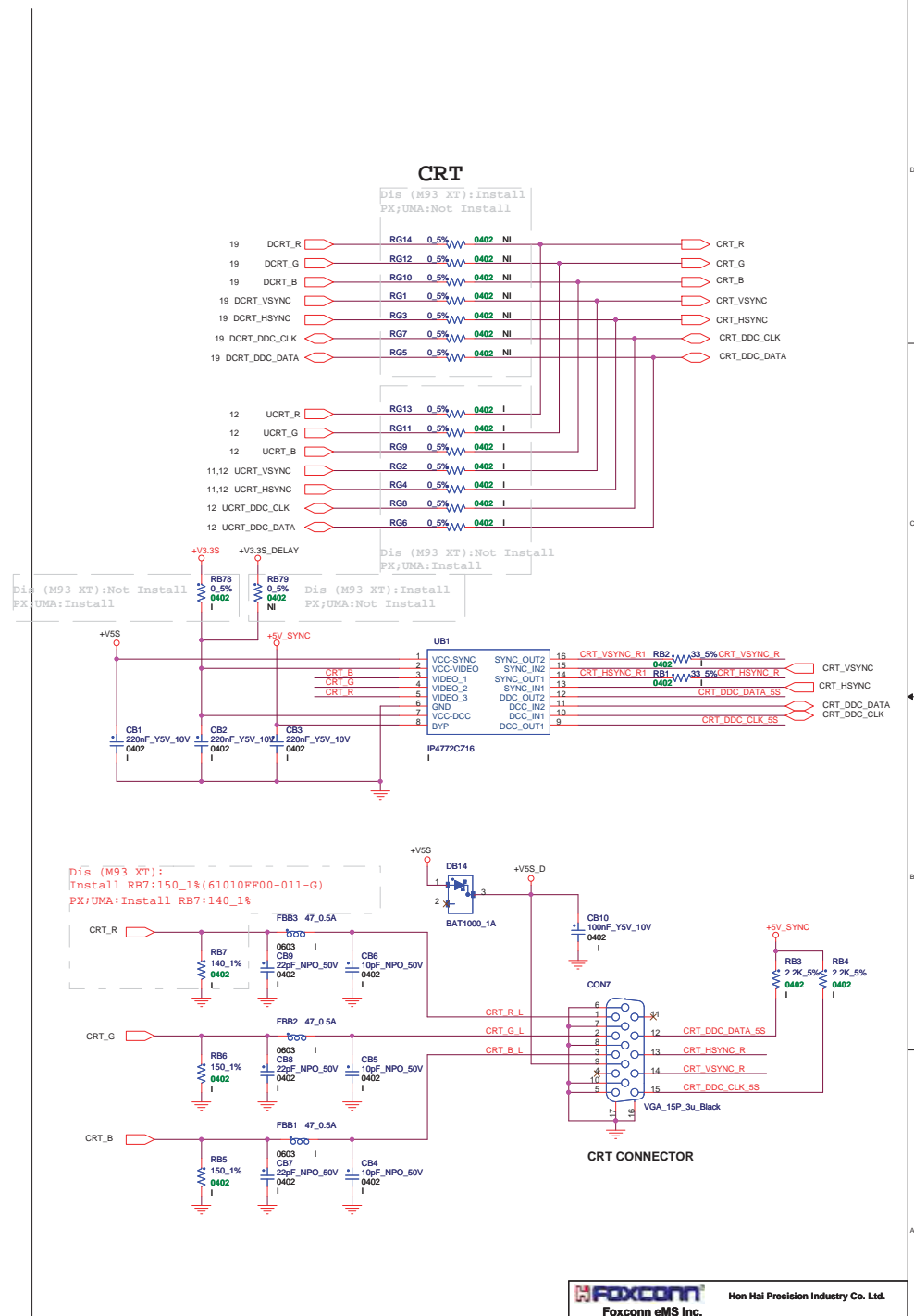
Power pin current  
max. 1300 mA (less 2ms)

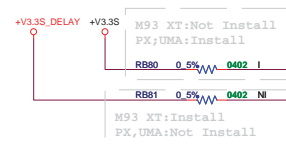
## HDD/ODD Status LED

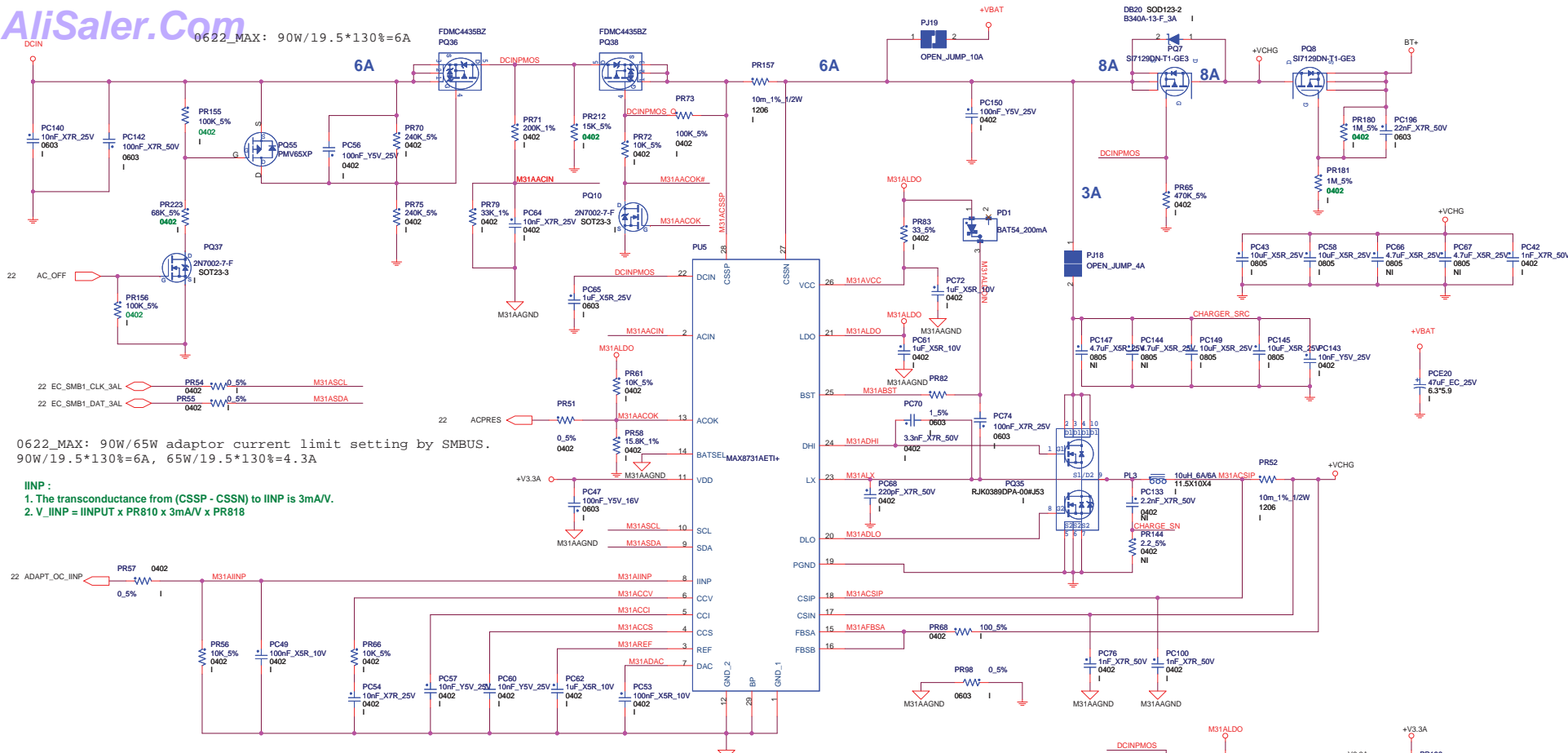


D3 mode: (R:0 ohm ; C:NC)  
If user remove memory card from socket, RTS5159 will terminate USB bus connection and enter D3 (power saving) state.

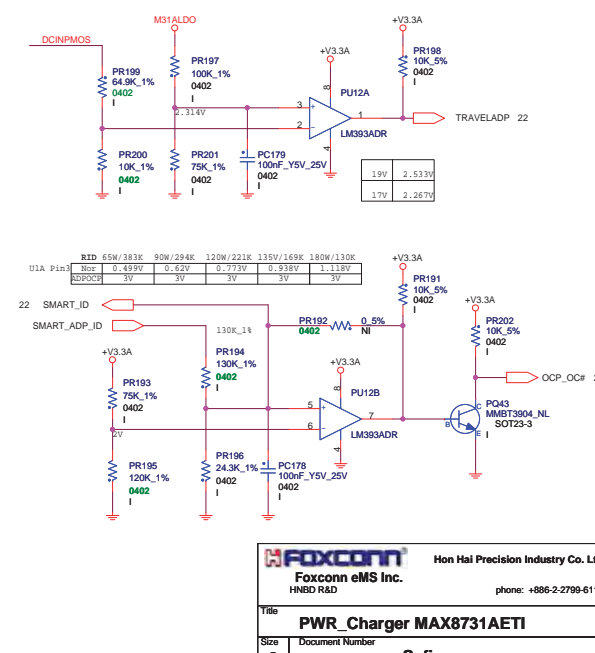
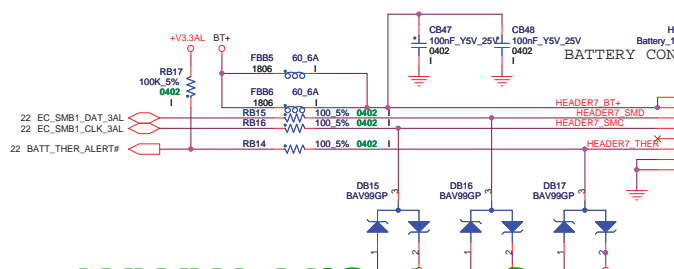
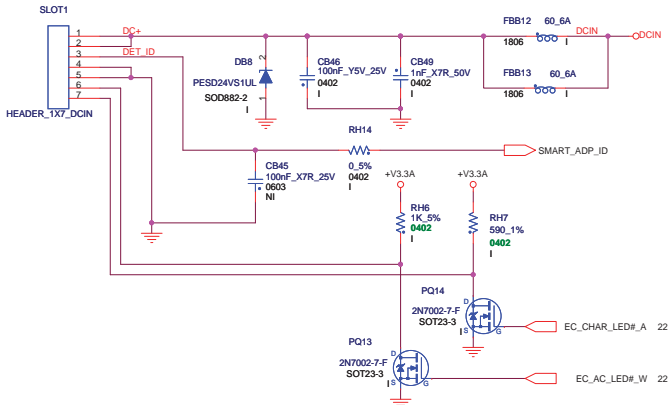






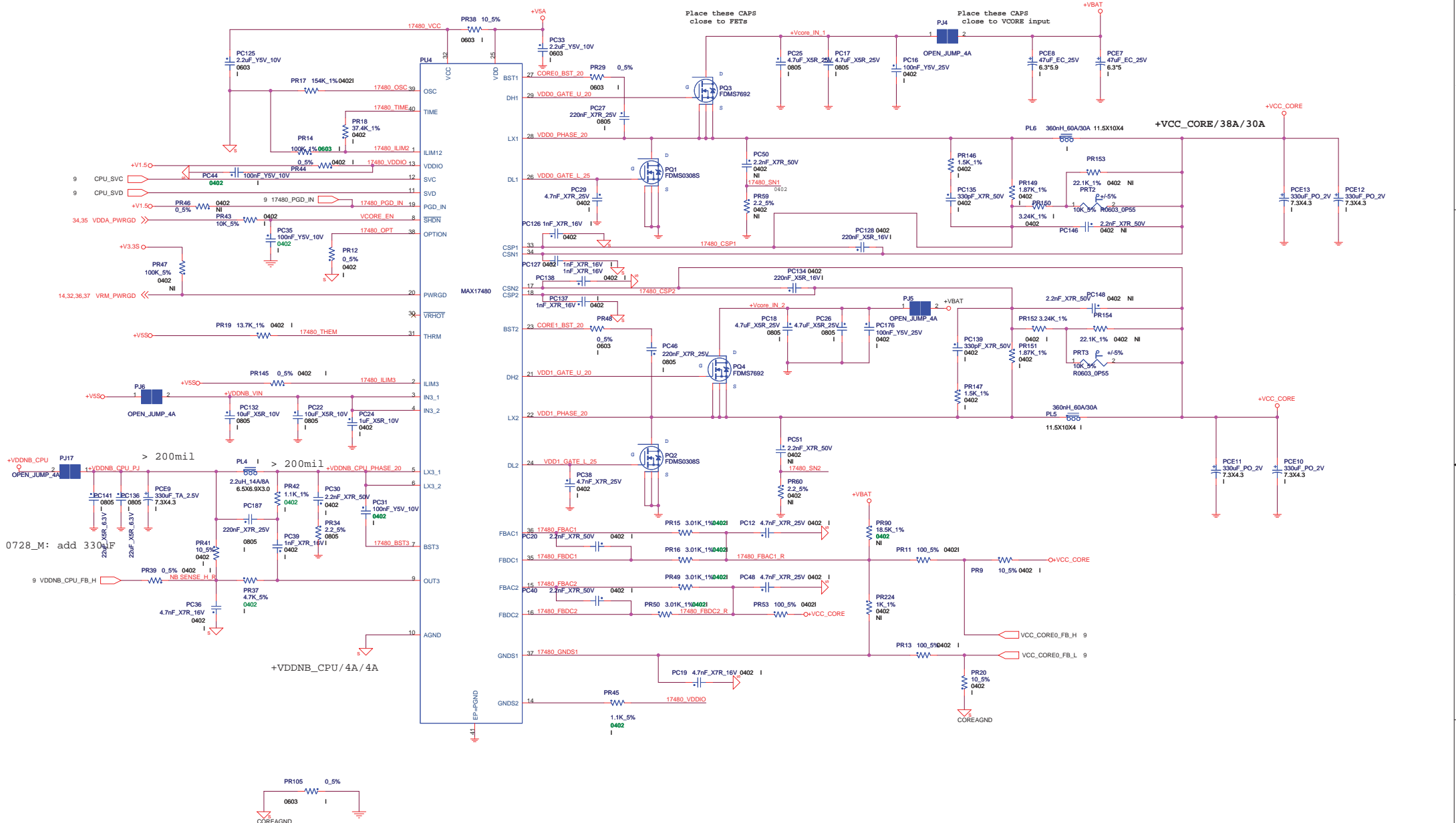


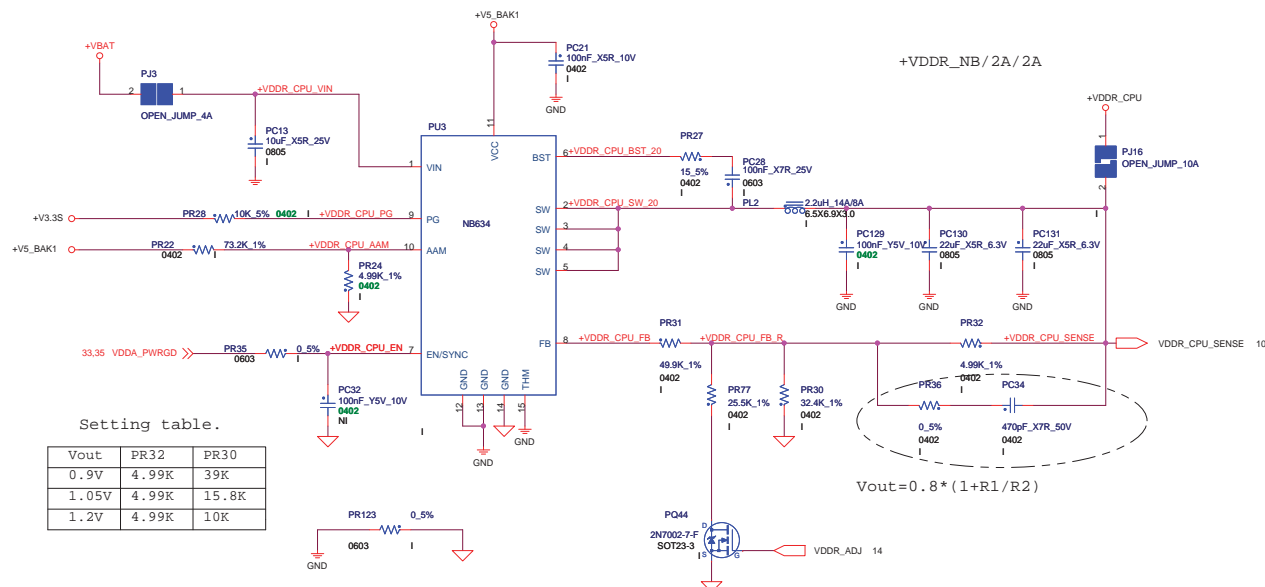
ADAPTOR In CON.





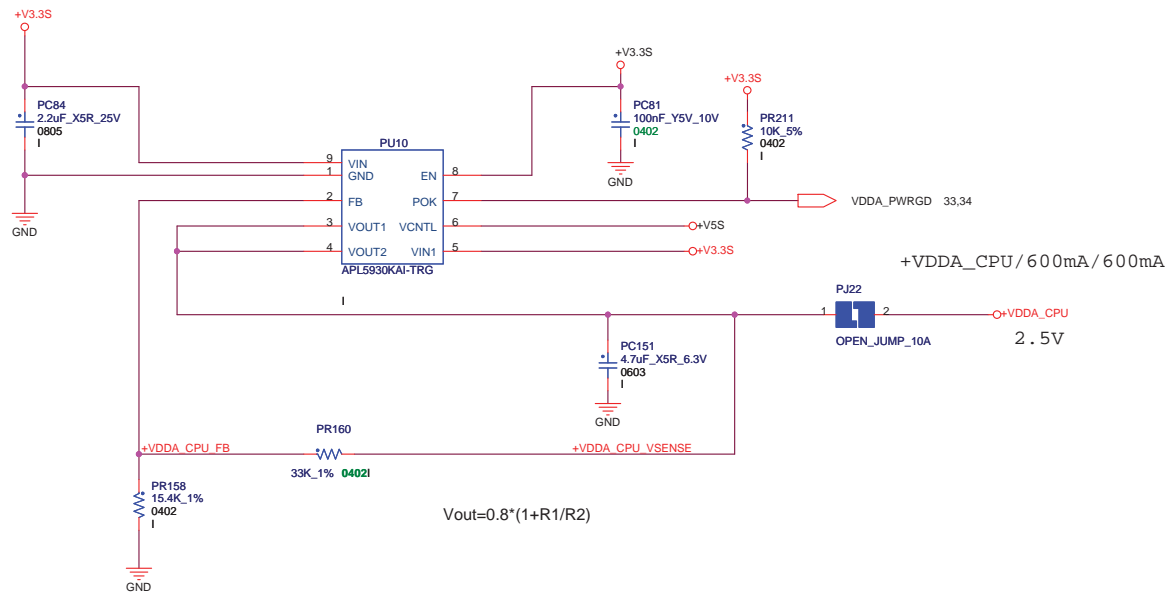


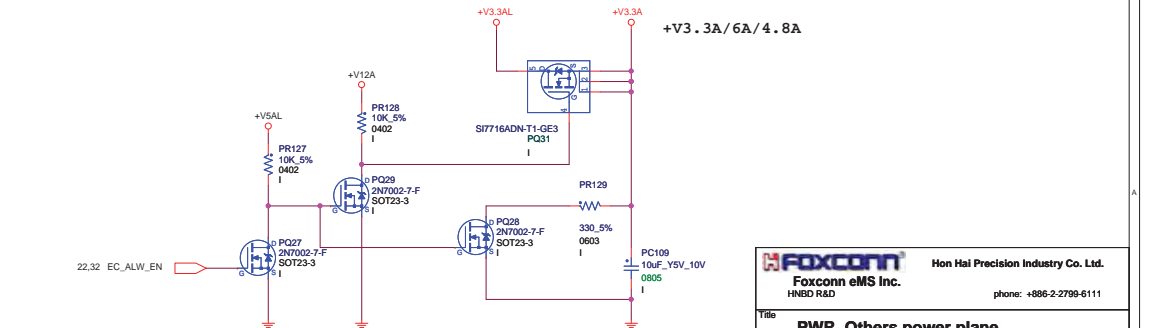
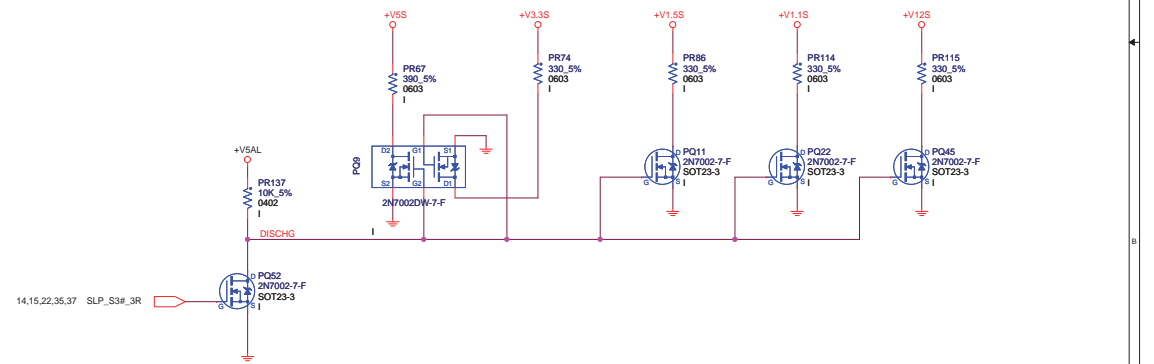
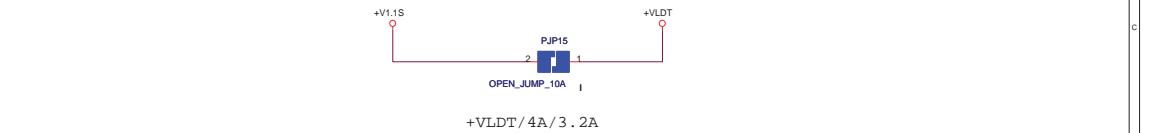
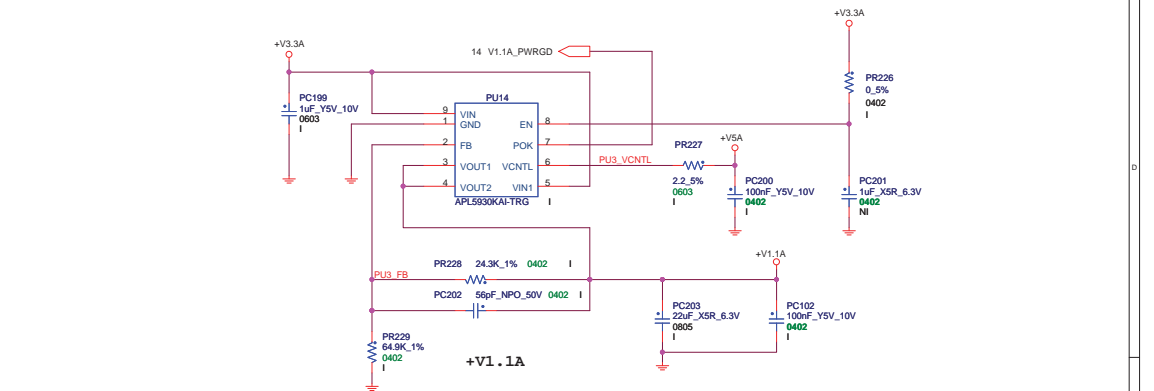
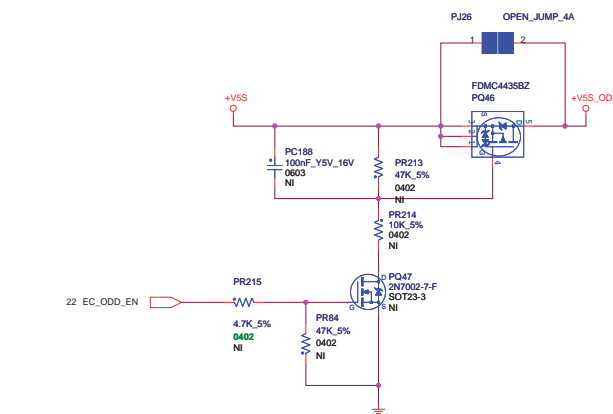
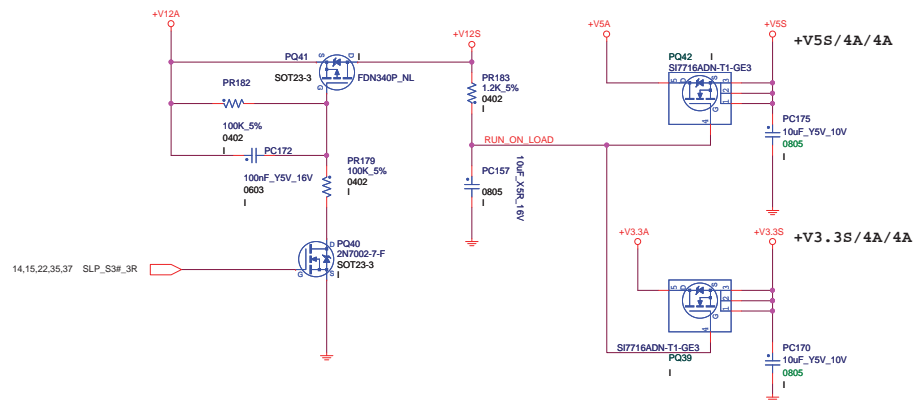
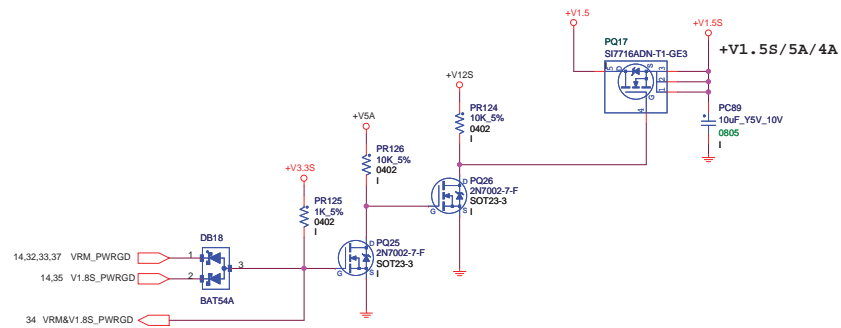


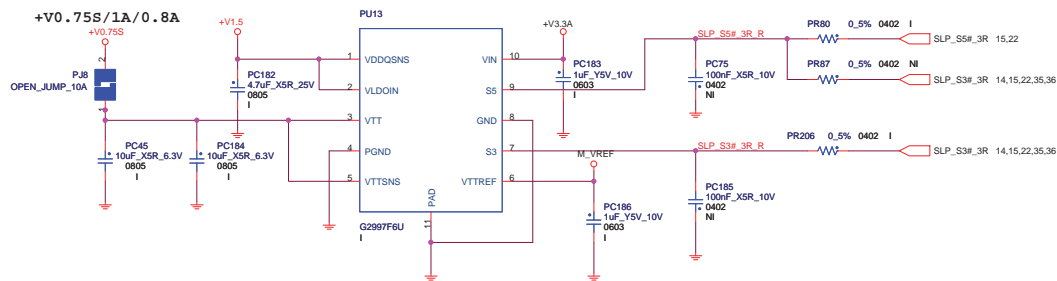


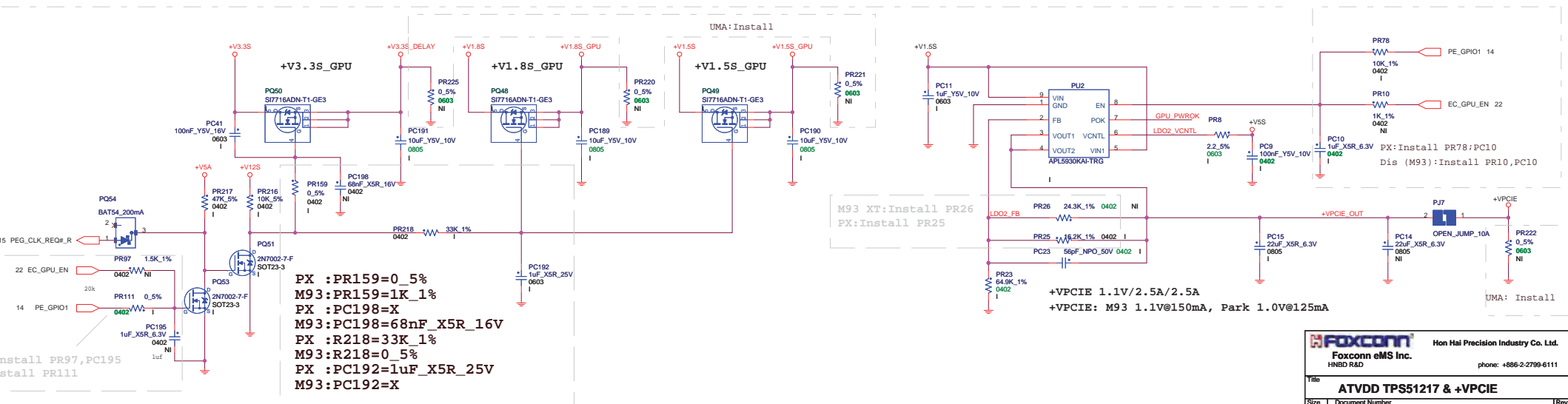
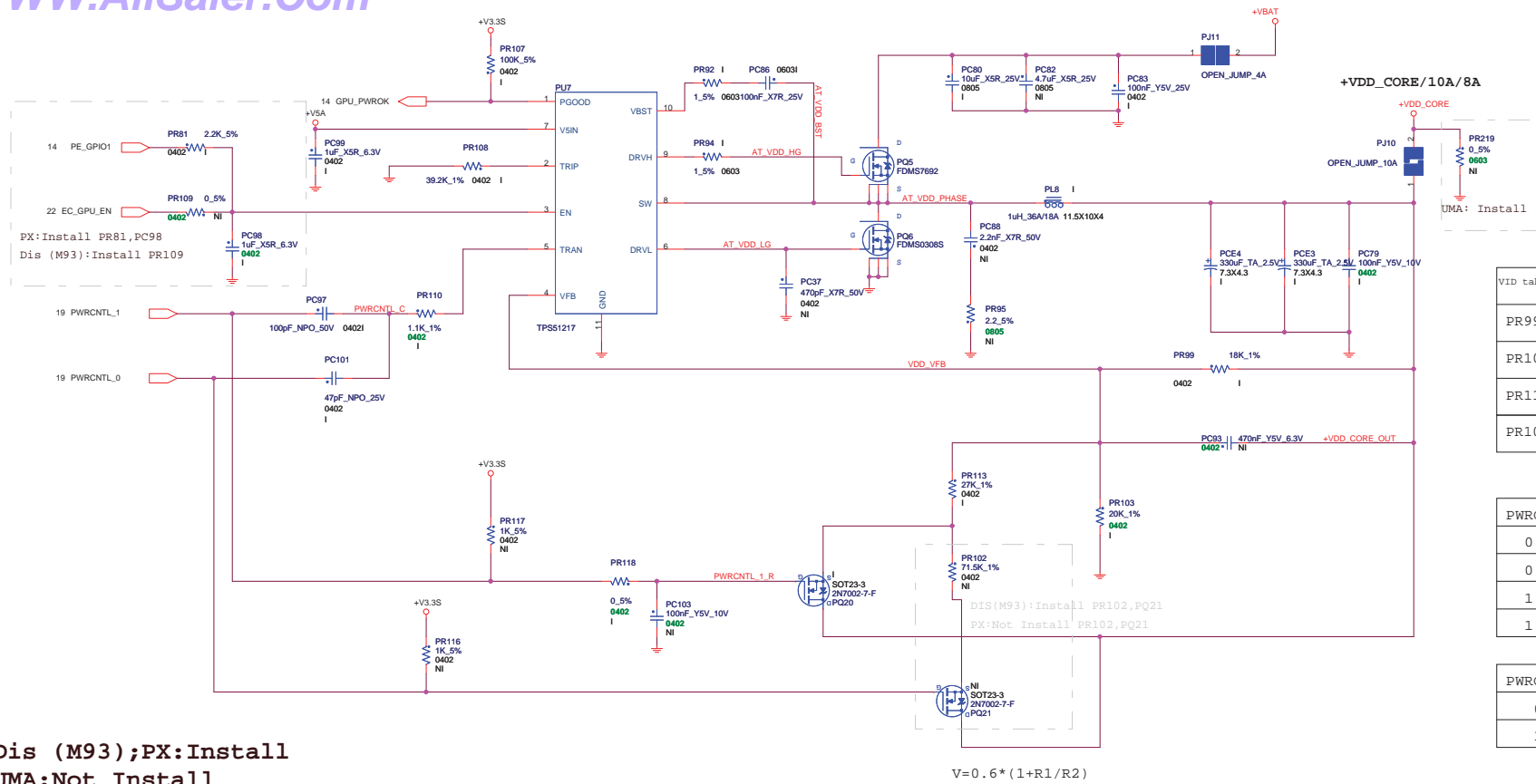
Setting table.

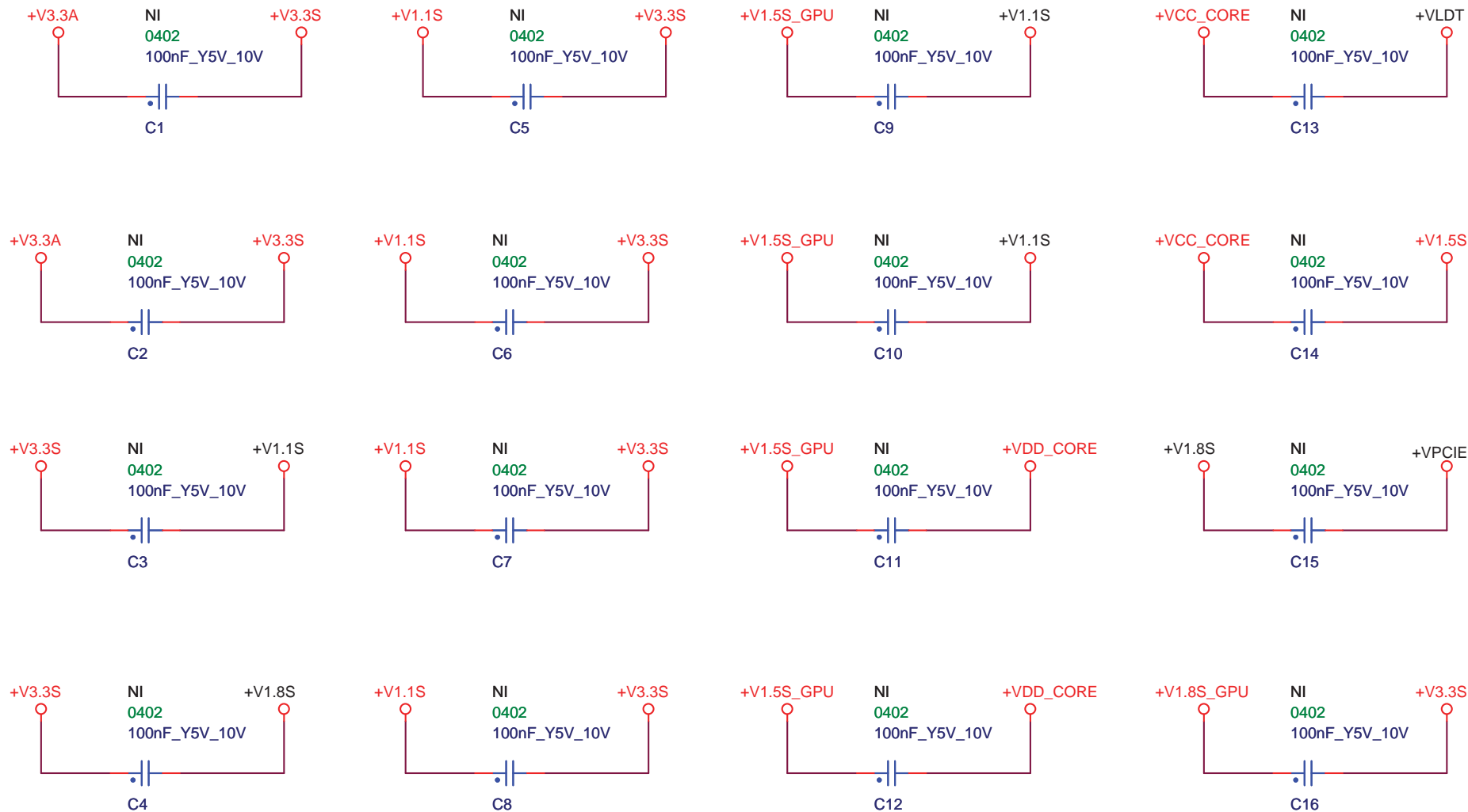
Vout	PR32	PR30
0.9V	4.99K	39K
1.05V	4.99K	15.8K
1.2V	4.99K	10K






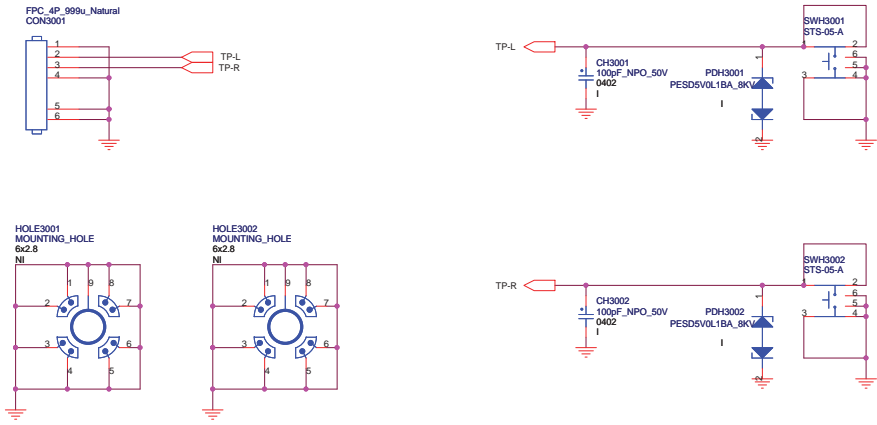




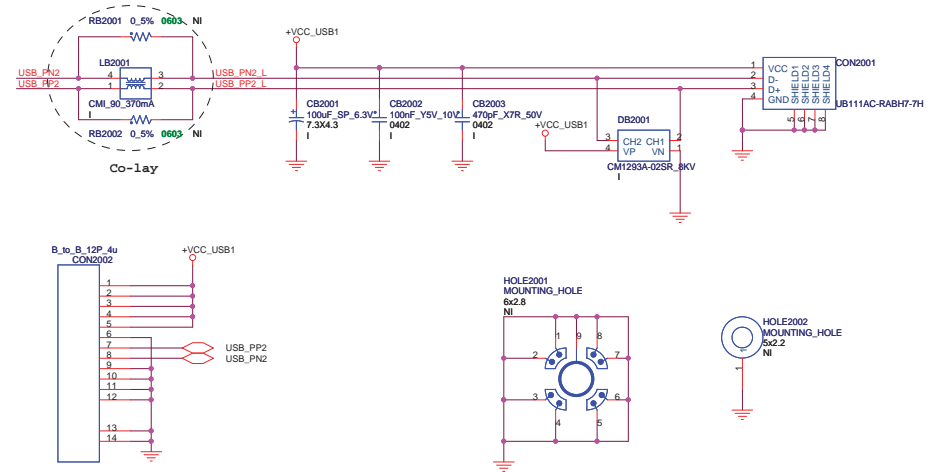


Only for 6 layer M/B use

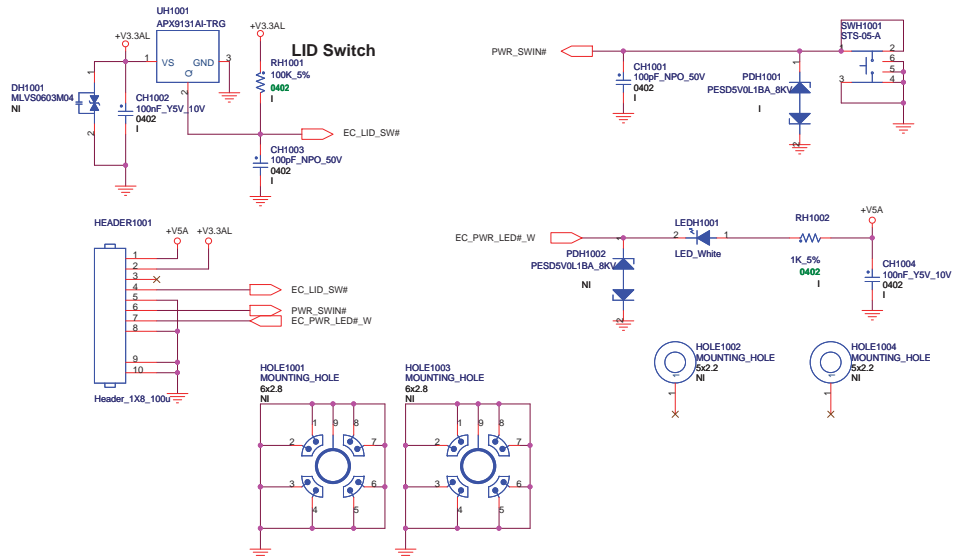
		Hon Hai Precision Industry Co. Ltd.	
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HNBD R&D		phone: +886-2-2799-6111	
Title			
SYSTEM BLOCK DIAGRAM			
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A	Safina		MV
Page Modified: Wednesday, April 07, 2010		18:49:16 (UTC/GMT)	Sheet 39 of 39



SW Board



USB Board



Power Board